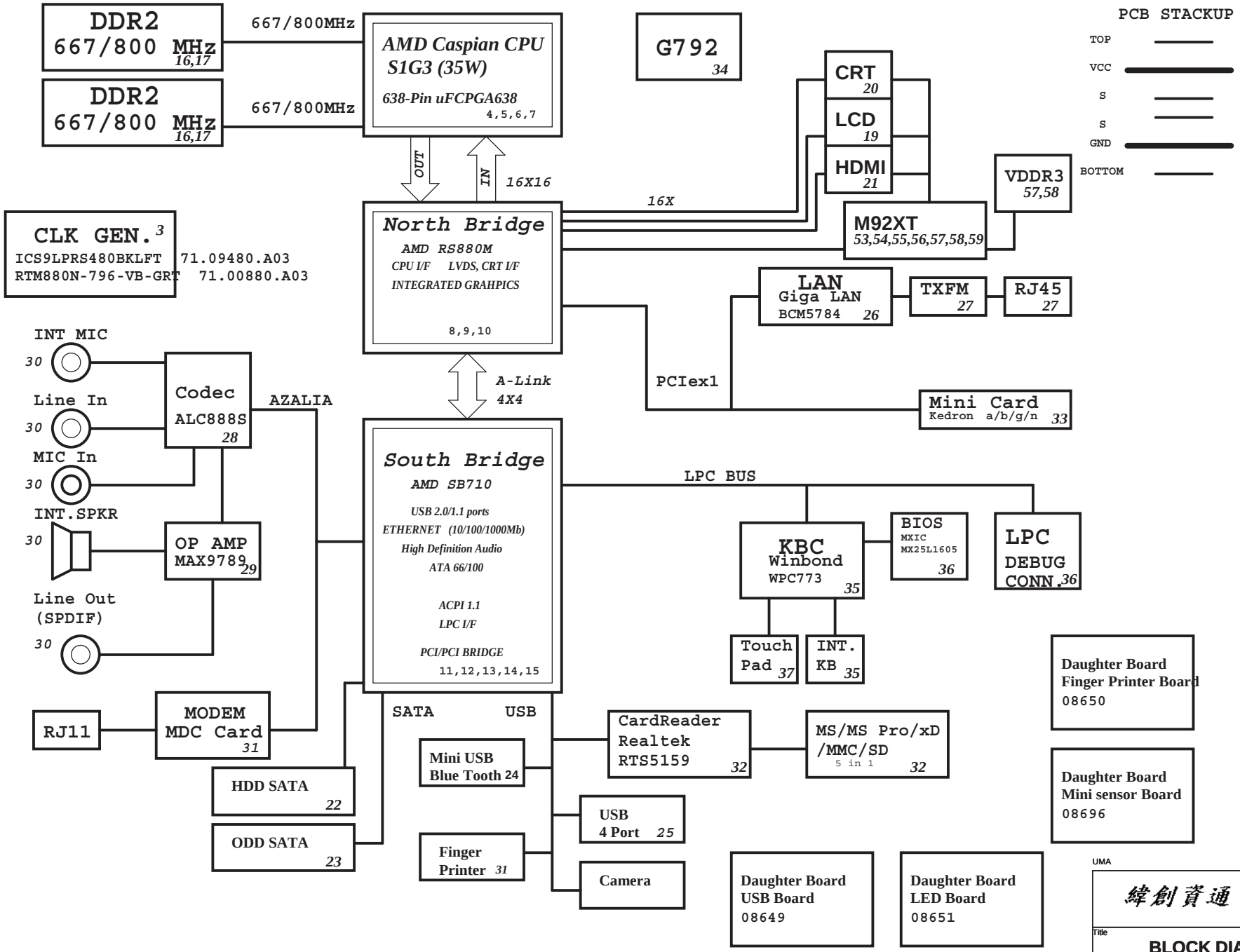
JV71-TR Block Diagram

Project code: 91.4FP01.001
PCB P/N : 48.4FP02.0SB
REVISION : 09243-SB



PCB STACKUP

TOP	
VCC	
S	
S	
GND	
BOTTOM	

SYSTEM DC/DC RT8205A 46

INPUTS	OUTPUTS
DCBATOUT	5V_S5(6A) 3D3V_S5(6A)

SYSTEM DC/DC TPS51124 47

INPUTS	OUTPUTS
DCBATOUT	1D1V_S0(7.5A) 1D2V_S0(4A)

SYSTEM DC/DC RT8209B 48

INPUTS	OUTPUTS
DCBATOUT	1D8V_S3(11A)

RT9025 49

5V_S5	1D1V_M92

RT9161 49

3D3V_S0	2D5V_S0 (200mA)

G957 49

3D3V_S0	1D5V_S0 (1A)

G9161 49

3D3V_S5	1D2V_S5 (400mA)

CHARGER MAX8731 50

INPUTS	OUTPUTS
DCBATOUT	CHG_PWR 18V 6.0A UP+5V 5V 100mA

CPU DC/DC ISL6265HR 45

INPUTS	OUTPUTS
DCBATOUT	VCC_CORE_S0_0 0~1.55V 18A VCC_CORE_S0_1 0~1.55V 18A VDDNB 0~1.55V 18A

UMA

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

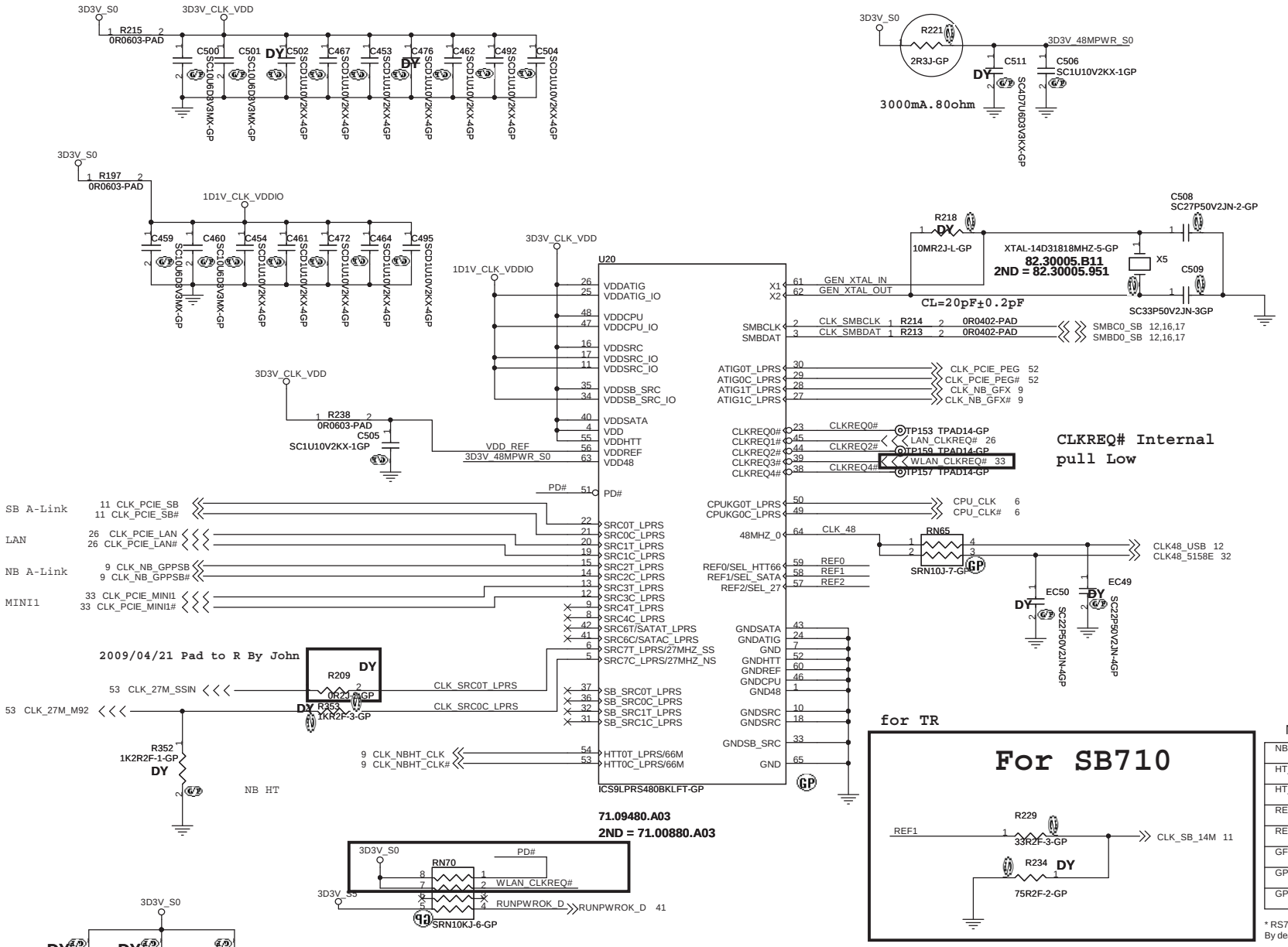
Title: BLOCK DIAGRAM

Size	Document Number	Rev
A3	JV71-TR	SB

Date: Monday, July 06, 2009 Sheet 1 of 61

UMA

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	**USB/PCIE Routing**	
Size A3	Document Number **JV71-TR**	Rev **SA**
Date: Monday, July 06, 2009	Sheet 2 of 61	



Due to PLL issue on current clock chip, the SBlink clock need to come from SRC clocks for RS740 and RS780. Future clock chip revision will fix this.

Clock chip has internal serial terminations for differencial pairs, external resistors are reserved for debug purpose.

SEL_27 REF2	1	27MHz non-spreading singled clock on pin 5 and 27MHz spread clock on pin 6
	0 *	100MHz differential spreading SRC clock
SEL_SATA REF1	1	100MHz non-spreading differential SATA clock
	0 *	100MHz differential spreading SRC clock
SEL_HTT66 REF0	1	66MHz 3.3V single ended HTT clock
	0 *	100MHz differential HTT clock

CPU_CLK(200MHz)

	OSC_14M_NB
RS780M	1.1V 158R/90.9R

NB CLOCK INPUT TABLE

NB CLOCKS	RS740	RX780	RS780
HT_REFCLKP	66M SE(SINGLE END)	100M DIFF	100M DIFF
HT_REFCLKN	NC	100M DIFF	100M DIFF
REFCLK_P	14M SE (3.3V)	14M SE (1.8V)	14M SE (1.1V)
REFCLK_N	NC	NC	vref
GFX_REFCLK	100M DIFF	100M DIFF	100M DIFF(IN/OUT)*
GPP_REFCLK	NC	100M DIFF	NC or 100M DIFF OUTPUT
GPPSB_REFCLK	100M DIFF	100M DIFF	100M DIFF

* RS780 can be used as clock buffer to output two PCIE referecence clocks
By deault, chip will configured as input mode, BIOS can program it to output mode.

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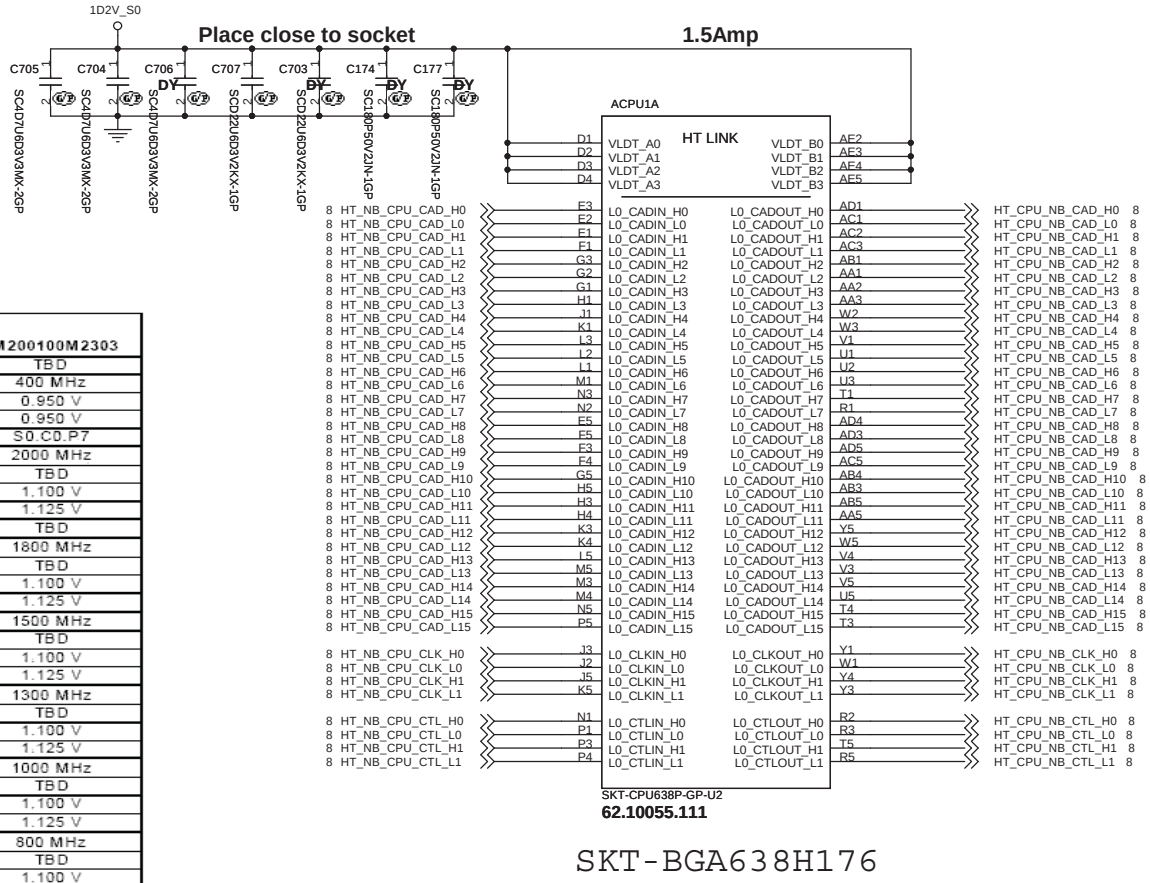
Title: CLKGEN_ICS9LPRS480

Size: A3 | Document Number: JV71-TR | Rev: SB

Date: Monday, July 06, 2009 | Sheet 3 of 61



SKT-BGA638H176

State	Specification	Notes	2M200100M2303
S0.C0.Px	Tcase Max	3	TBD
	NB COF	1	400 MHz
	VID_VDDNB Min	2	0.950 V
	VID_VDDNB Max	2	0.950 V
	Startup P-state		S0.C0.P7
S0.C0.P0	CPU COF	1	2000 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
	IDD Max	3	TBD
S0.C0.P1	CPU COF	1	1800 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
S0.C0.P2	CPU COF	1	1500 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
S0.C0.P3	CPU COF	1	1300 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
S0.C0.P4	CPU COF	1	1000 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
S0.C0.P5	CPU COF	1	800 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
S0.C0.P6	CPU COF	1	500 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
S0.C0.P7	CPU COF	1	300 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V

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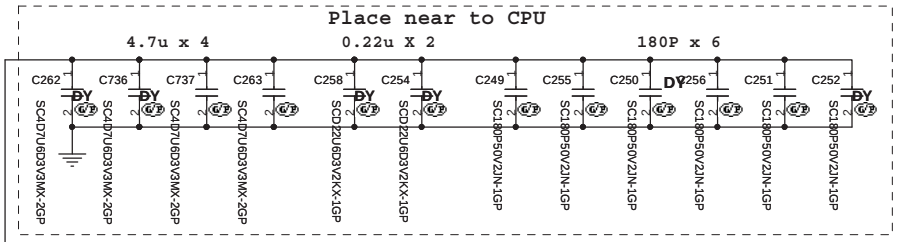
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU HT LINK I/F (1/4)

Size: A3 | Document Number: JV71-TR | Rev: SA

Date: Monday, July 06, 2009 | Sheet 4 of 61



750 mA

0D9V_S3

ACPU1B

MEM:CMD/CTRL/CLK

		D10	VTT1	W10	
		C10	VTT2	AC10	
		B10	VTT3	AB10	
		AD10	VTT4	AA10	
				VTT5	
				VTT6	
				VTT7	
				VTT8	
				VTT9	
				A10	
1D8V_S3	R381 39D2R2F-L-GP				
		MEMZP	AE10	MEMZP	
		MEMZN	AE10	MEMZN	
	R383 39D2R2F-L-GPTP111	MEM_RSVD_M1	H16	RSVD_M1	
				MEMVREF	W17
				VTT_SENSE	Y10 VTT_SENSE 1 TP106TPAD14-GP
				RSVD_M2	B18 MEM_RSVD_M2 1 TP112
16,18 MEM_MA0_ODT0		T19	MA0_ODT0	MB0_ODT0	W26 MEM_MB0_ODT0 17,18
16,18 MEM_MA0_ODT1		V22	MA0_ODT1	MB0_ODT1	W23 MEM_MB0_ODT1 17,18
		U21	MA1_ODT0	MB1_ODT0	Y26
		V19	MA1_ODT1		
16,18 MEM_MA0_CS#0		T20	MA0_CS_L0	MB0_CS_L0	V26 MEM_MB0_CS#0 17,18
16,18 MEM_MA0_CS#1		U19	MA0_CS_L1	MB0_CS_L1	W25 MEM_MB0_CS#1 17,18
		U20	MA1_CS_L0	MB1_CS_L0	U22
		V20	MA1_CS_L1		
16,18 MEM_MA_CKE0		J22	MA_CKE0	MB_CKE0	J25 MEM_MB_CKE0 17,18
16,18 MEM_MA_CKE1		J20	MA_CKE1	MB_CKE1	H26 MEM_MB_CKE1 17,18
		N19	MA_CLK_H5	MB_CLK_H5	P22
		N20	MA_CLK_L5	MB_CLK_L5	R22
16 MEM_MA_CLK0_P		E16	MA_CLK_H1	MB_CLK_H1	A17 MEM_MB_CLK0_P 17
16 MEM_MA_CLK0_N		F16	MA_CLK_L1	MB_CLK_L1	A18 MEM_MB_CLK0_N 17
16 MEM_MA_CLK1_P		Y16	MA_CLK_H7	MB_CLK_H7	AF18 MEM_MB_CLK1_P 17
16 MEM_MA_CLK1_N		AA16	MA_CLK_L7	MB_CLK_L7	AE17 MEM_MB_CLK1_N 17
		P19	MA_CLK_H4	MB_CLK_H4	R26
		P20	MA_CLK_L4	MB_CLK_L4	R25
16,18 MEM_MA_ADD0		N21	MA_ADD0	MB_ADD0	P24 MEM_MB_ADD0 17,18
16,18 MEM_MA_ADD1		M20	MA_ADD1	MB_ADD1	N24 MEM_MB_ADD1 17,18
16,18 MEM_MA_ADD2		N22	MA_ADD2	MB_ADD2	P26 MEM_MB_ADD2 17,18
16,18 MEM_MA_ADD3		M19	MA_ADD3	MB_ADD3	N23 MEM_MB_ADD3 17,18
16,18 MEM_MA_ADD4		M22	MA_ADD4	MB_ADD4	N26 MEM_MB_ADD4 17,18
16,18 MEM_MA_ADD5		L20	MA_ADD5	MB_ADD5	L23 MEM_MB_ADD5 17,18
16,18 MEM_MA_ADD6		M24	MA_ADD6	MB_ADD6	N25 MEM_MB_ADD6 17,18
16,18 MEM_MA_ADD7		L21	MA_ADD7	MB_ADD7	L24 MEM_MB_ADD7 17,18
16,18 MEM_MA_ADD8		L19	MA_ADD8	MB_ADD8	M26 MEM_MB_ADD8 17,18
16,18 MEM_MA_ADD9		K22	MA_ADD9	MB_ADD9	K26 MEM_MB_ADD9 17,18
16,18 MEM_MA_ADD10		R21	MA_ADD10	MB_ADD10	T26 MEM_MB_ADD10 17,18
16,18 MEM_MA_ADD11		L22	MA_ADD11	MB_ADD11	L26 MEM_MB_ADD11 17,18
16,18 MEM_MA_ADD12		K20	MA_ADD12	MB_ADD12	L25 MEM_MB_ADD12 17,18
16,18 MEM_MA_ADD13		V24	MA_ADD13	MB_ADD13	W24 MEM_MB_ADD13 17,18
16,18 MEM_MA_ADD14		K24	MA_ADD14	MB_ADD14	J23 MEM_MB_ADD14 17,18
16,18 MEM_MA_ADD15		K19	MA_ADD15	MB_ADD15	J24 MEM_MB_ADD15 17,18
16,18 MEM_MA_BANK0		R20	MA_BANK0	MB_BANK0	R24 MEM_MB_BANK0 17,18
16,18 MEM_MA_BANK1		R23	MA_BANK1	MB_BANK1	U26 MEM_MB_BANK1 17,18
16,18 MEM_MA_BANK2		J21	MA_BANK2	MB_BANK2	J26 MEM_MB_BANK2 17,18
16,18 MEM_MA_RAS#		R19	MA_RAS_L	MB_RAS_L	U25 MEM_MB_RAS# 17,18
16,18 MEM_MA_CAS#		T22	MA_CAS_L	MB_CAS_L	U24 MEM_MB_CAS# 17,18
16,18 MEM_MA_WE#		T24	MA_WE_L	MB_WE_L	U23 MEM_MB_WE# 17,18

SKT-CPU638P-GP-U2

62.10055.111

CLOSE TO CPU

1D8V_S3

C397 SCD1U10V2KX-4GP

VREF_DDR_CLAW

RN48 SRN1KJ-7-GP

C391 SC1KP50V2KX-XGP

C388 SCD1U10V2KX-4GP

ACPU1C

MEM:DATA

16 MEM_MA_DATA0	G12	MA_DATA0	MB_DATA0	C11	MEM_MB_DATA0 17
16 MEM_MA_DATA1	F12	MA_DATA1	MB_DATA1	A11	MEM_MB_DATA1 17
16 MEM_MA_DATA2	H14	MA_DATA2	MB_DATA2	A14	MEM_MB_DATA2 17
16 MEM_MA_DATA3	G14	MA_DATA3	MB_DATA3	B14	MEM_MB_DATA3 17
16 MEM_MA_DATA4	H11	MA_DATA4	MB_DATA4	G11	MEM_MB_DATA4 17
16 MEM_MA_DATA5	H12	MA_DATA5	MB_DATA5	E11	MEM_MB_DATA5 17
16 MEM_MA_DATA6	C13	MA_DATA6	MB_DATA6	D12	MEM_MB_DATA6 17
16 MEM_MA_DATA7	E13	MA_DATA7	MB_DATA7	A13	MEM_MB_DATA7 17
16 MEM_MA_DATA8	H15	MA_DATA8	MB_DATA8	A15	MEM_MB_DATA8 17
16 MEM_MA_DATA9	F15	MA_DATA9	MB_DATA9	A16	MEM_MB_DATA9 17
16 MEM_MA_DATA10	E17	MA_DATA10	MB_DATA10	A19	MEM_MB_DATA10 17
16 MEM_MA_DATA11	H17	MA_DATA11	MB_DATA11	A20	MEM_MB_DATA11 17
16 MEM_MA_DATA12	E14	MA_DATA12	MB_DATA12	C14	MEM_MB_DATA12 17
16 MEM_MA_DATA13	F14	MA_DATA13	MB_DATA13	D14	MEM_MB_DATA13 17
16 MEM_MA_DATA14	C17	MA_DATA14	MB_DATA14	C18	MEM_MB_DATA14 17
16 MEM_MA_DATA15	G17	MA_DATA15	MB_DATA15	D18	MEM_MB_DATA15 17
16 MEM_MA_DATA16	G18	MA_DATA16	MB_DATA16	D20	MEM_MB_DATA16 17
16 MEM_MA_DATA17	C19	MA_DATA17	MB_DATA17	A21	MEM_MB_DATA17 17
16 MEM_MA_DATA18	D22	MA_DATA18	MB_DATA18	D24	MEM_MB_DATA18 17
16 MEM_MA_DATA19	E20	MA_DATA19	MB_DATA19	C25	MEM_MB_DATA19 17
16 MEM_MA_DATA20	E18	MA_DATA20	MB_DATA20	B20	MEM_MB_DATA20 17
16 MEM_MA_DATA21	F18	MA_DATA21	MB_DATA21	C20	MEM_MB_DATA21 17
16 MEM_MA_DATA22	B22	MA_DATA22	MB_DATA22	B24	MEM_MB_DATA22 17
16 MEM_MA_DATA23	C23	MA_DATA23	MB_DATA23	C24	MEM_MB_DATA23 17
16 MEM_MA_DATA24	F20	MA_DATA24	MB_DATA24	E23	MEM_MB_DATA24 17
16 MEM_MA_DATA25	F22	MA_DATA25	MB_DATA25	E24	MEM_MB_DATA25 17
16 MEM_MA_DATA26	H24	MA_DATA26	MB_DATA26	G25	MEM_MB_DATA26 17
16 MEM_MA_DATA27	J19	MA_DATA27	MB_DATA27	G26	MEM_MB_DATA27 17
16 MEM_MA_DATA28	E21	MA_DATA28	MB_DATA28	C26	MEM_MB_DATA28 17
16 MEM_MA_DATA29	F22	MA_DATA29	MB_DATA29	D26	MEM_MB_DATA29 17
16 MEM_MA_DATA30	H20	MA_DATA30	MB_DATA30	G23	MEM_MB_DATA30 17
16 MEM_MA_DATA31	H22	MA_DATA31	MB_DATA31	G24	MEM_MB_DATA31 17
16 MEM_MA_DATA32	Y24	MA_DATA32	MB_DATA32	AA24	MEM_MB_DATA32 17
16 MEM_MA_DATA33	AB24	MA_DATA33	MB_DATA33	AA23	MEM_MB_DATA33 17
16 MEM_MA_DATA34	AB22	MA_DATA34	MB_DATA34	AD24	MEM_MB_DATA34 17
16 MEM_MA_DATA35	AA21	MA_DATA35	MB_DATA35	AE24	MEM_MB_DATA35 17
16 MEM_MA_DATA36	W22	MA_DATA36	MB_DATA36	AA26	MEM_MB_DATA36 17
16 MEM_MA_DATA37	W21	MA_DATA37	MB_DATA37	AA25	MEM_MB_DATA37 17
16 MEM_MA_DATA38	Y22	MA_DATA38	MB_DATA38	AD26	MEM_MB_DATA38 17
16 MEM_MA_DATA39	AA22	MA_DATA39	MB_DATA39	AE25	MEM_MB_DATA39 17
16 MEM_MA_DATA40	Y20	MA_DATA40	MB_DATA40	AC22	MEM_MB_DATA40 17
16 MEM_MA_DATA41	AA20	MA_DATA41	MB_DATA41	AD22	MEM_MB_DATA41 17
16 MEM_MA_DATA42	AA18	MA_DATA42	MB_DATA42	AE20	MEM_MB_DATA42 17
16 MEM_MA_DATA43	AB18	MA_DATA43	MB_DATA43	AF20	MEM_MB_DATA43 17
16 MEM_MA_DATA44	AB21	MA_DATA44	MB_DATA44	AF24	MEM_MB_DATA44 17
16 MEM_MA_DATA45	AD21	MA_DATA45	MB_DATA45	AF23	MEM_MB_DATA45 17
16 MEM_MA_DATA46	AD19	MA_DATA46	MB_DATA46	AC20	MEM_MB_DATA46 17
16 MEM_MA_DATA47	Y18	MA_DATA47	MB_DATA47	AD20	MEM_MB_DATA47 17
16 MEM_MA_DATA48	AD17	MA_DATA48	MB_DATA48	AD18	MEM_MB_DATA48 17
16 MEM_MA_DATA49	W16	MA_DATA49	MB_DATA49	AF18	MEM_MB_DATA49 17
16 MEM_MA_DATA50	W14	MA_DATA50	MB_DATA50	AC14	MEM_MB_DATA50 17
16 MEM_MA_DATA51	Y14	MA_DATA51	MB_DATA51	AD14	MEM_MB_DATA51 17
16 MEM_MA_DATA52	Y17	MA_DATA52	MB_DATA52	AF19	MEM_MB_DATA52 17
16 MEM_MA_DATA53	AB17	MA_DATA53	MB_DATA53	AC18	MEM_MB_DATA53 17
16 MEM_MA_DATA54	AB15	MA_DATA54	MB_DATA54	AF16	MEM_MB_DATA54 17
16 MEM_MA_DATA55	AD15	MA_DATA55	MB_DATA55	AE15	MEM_MB_DATA55 17
16 MEM_MA_DATA56	AB13	MA_DATA56	MB_DATA56	AF13	MEM_MB_DATA56 17
16 MEM_MA_DATA57	AD13	MA_DATA57	MB_DATA57	AC12	MEM_MB_DATA57 17
16 MEM_MA_DATA58	Y12	MA_DATA58	MB_DATA58	AB11	MEM_MB_DATA58 17
16 MEM_MA_DATA59	W11	MA_DATA59	MB_DATA59	Y11	MEM_MB_DATA59 17
16 MEM_MA_DATA60	AB14	MA_DATA60	MB_DATA60	AE14	MEM_MB_DATA60 17
16 MEM_MA_DATA61	AA14	MA_DATA61	MB_DATA61	AF14	MEM_MB_DATA61 17
16 MEM_MA_DATA62	AB12	MA_DATA62	MB_DATA62	AF11	MEM_MB_DATA62 17
16 MEM_MA_DATA63	AA12	MA_DATA63	MB_DATA63	AD11	MEM_MB_DATA63 17
16 MEM_MA_DM0	E12	MA_DM0	MB_DM0	A12	MEM_MB_DM0 17
16 MEM_MA_DM1	C15	MA_DM1	MB_DM1	B16	MEM_MB_DM1 17
16 MEM_MA_DM2	E19	MA_DM2	MB_DM2	A22	MEM_MB_DM2 17
16 MEM_MA_DM3	F24	MA_DM3	MB_DM3	E25	MEM_MB_DM3 17
16 MEM_MA_DM4	AC24	MA_DM4	MB_DM4	AB26	MEM_MB_DM4 17
16 MEM_MA_DM5	Y19	MA_DM5	MB_DM5	AE22	MEM_MB_DM5 17
16 MEM_MA_DM6	AB16	MA_DM6	MB_DM6	AC16	MEM_MB_DM6 17
16 MEM_MA_DM7	Y13	MA_DM7	MB_DM7	AD12	MEM_MB_DM7 17
16 MEM_MA_DQS0_P	G13	MA_DQS_H0	MB_DQS_H0	C12	MEM_MB_DQS0_P 17
16 MEM_MA_DQS0_N	H13	MA_DQS_L0	MB_DQS_L0	B12	MEM_MB_DQS0_N 17
16 MEM_MA_DQS1_P	G16	MA_DQS_H1	MB_DQS_H1	D16	MEM_MB_DQS1_P 17
16 MEM_MA_DQS1_N	G15	MA_DQS_L1	MB_DQS_L1	C16	MEM_MB_DQS1_N 17
16 MEM_MA_DQS2_P	C22	MA_DQS_H2	MB_DQS_H2	A24	MEM_MB_DQS2_P 17
16 MEM_MA_DQS2_N	C21	MA_DQS_L2	MB_DQS_L2	A23	MEM_MB_DQS2_N 17
16 MEM_MA_DQS3_P	G22	MA_DQS_H3	MB_DQS_H3	F26	MEM_MB_DQS3_P 17
16 MEM_MA_DQS3_N	G21	MA_DQS_L3	MB_DQS_L3	E26	MEM_MB_DQS3_N 17
16 MEM_MA_DQS4_P	AD23	MA_DQS_H4	MB_DQS_H4	AC25	MEM_MB_DQS4_P 17
16 MEM_MA_DQS4_N	AC23	MA_DQS_L4	MB_DQS_L4	AC26	MEM_MB_DQS4_N 17
16 MEM_MA_DQS5_P	AB19	MA_DQS_H5	MB_DQS_H5	AF21	MEM_MB_DQS5_P 17
16 MEM_MA_DQS5_N	AB20	MA_DQS_L5	MB_DQS_L5	AE22	MEM_MB_DQS5_N 17
16 MEM_MA_DQS6_P	Y15	MA_DQS_H6	MB_DQS_H6	AE16	MEM_MB_DQS6_P 17
16 MEM_MA_DQS6_N	W15	MA_DQS_L6	MB_DQS_L6	AD16	MEM_MB_DQS6_N 17
16 MEM_MA_DQS7_P	W12	MA_DQS_H7	MB_DQS_H7	AE12	MEM_MB_DQS7_P 17
16 MEM_MA_DQS7_N	W13	MA_DQS_L7	MB_DQS_L7	AE12	MEM_MB_DQS7_N 17

SKT-CPU638P-GP-U2

62.10055.111

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緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **CPU DDR (2/4)**

Size	Document Number	Rev
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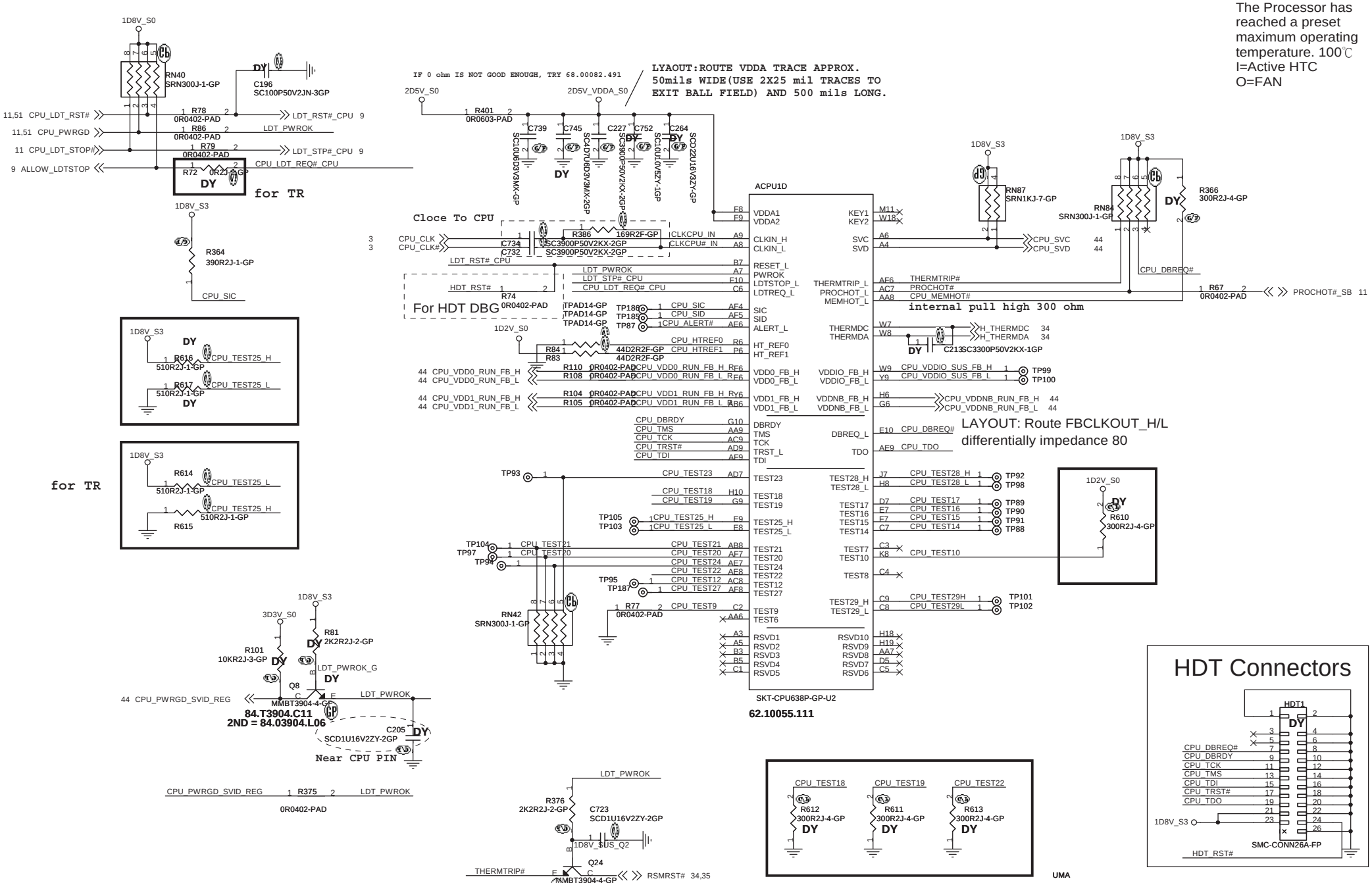
The Processor has reached a preset maximum operating temperature. 100℃
I=Active HTC
O=FAN



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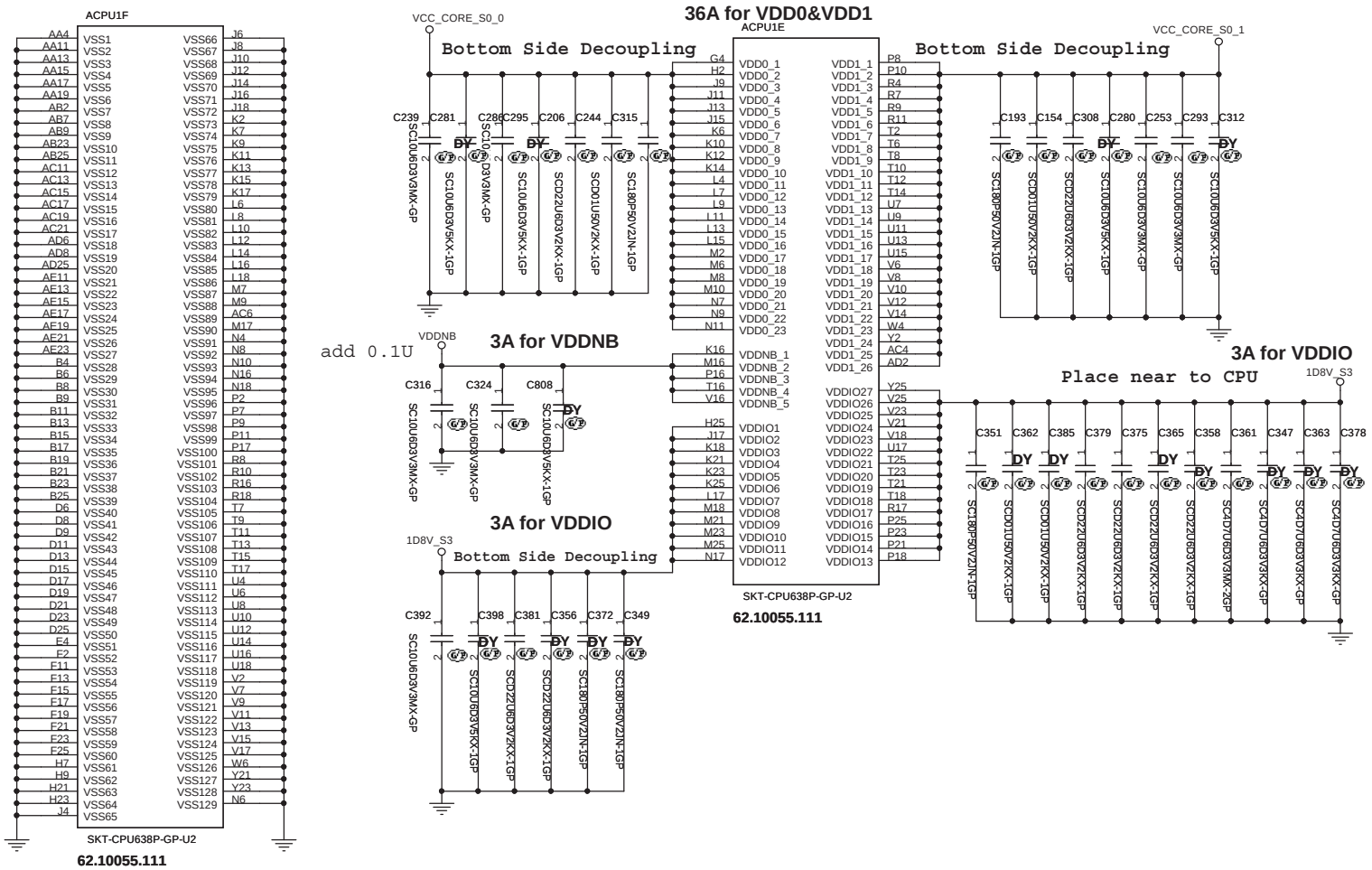
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **CPU_Control&Debug_(3/4)**

Size	Document Number	Rev
A3	JV71-TR	SA

Date: Monday, July 06, 2009 Sheet 6 of 61



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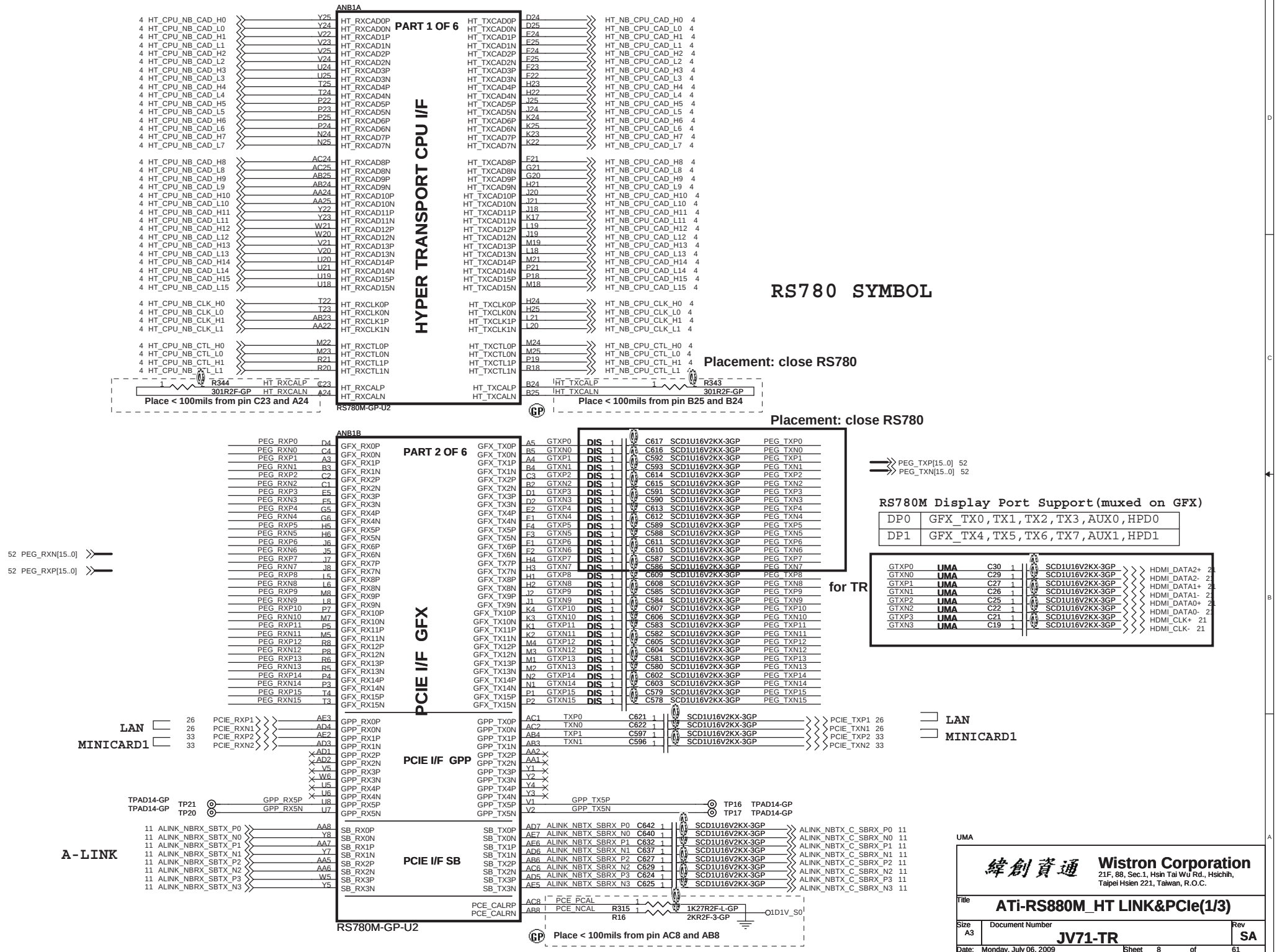
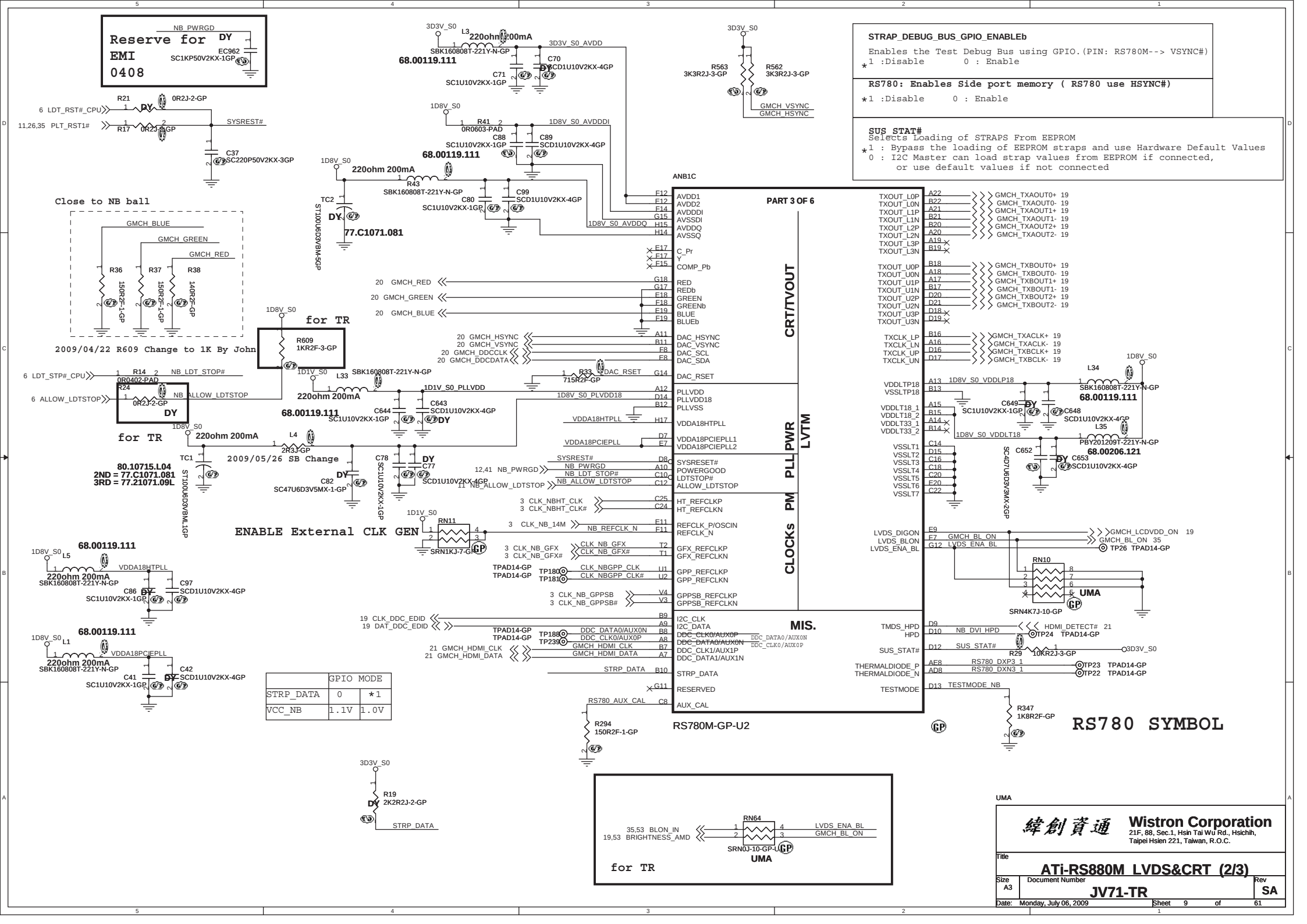
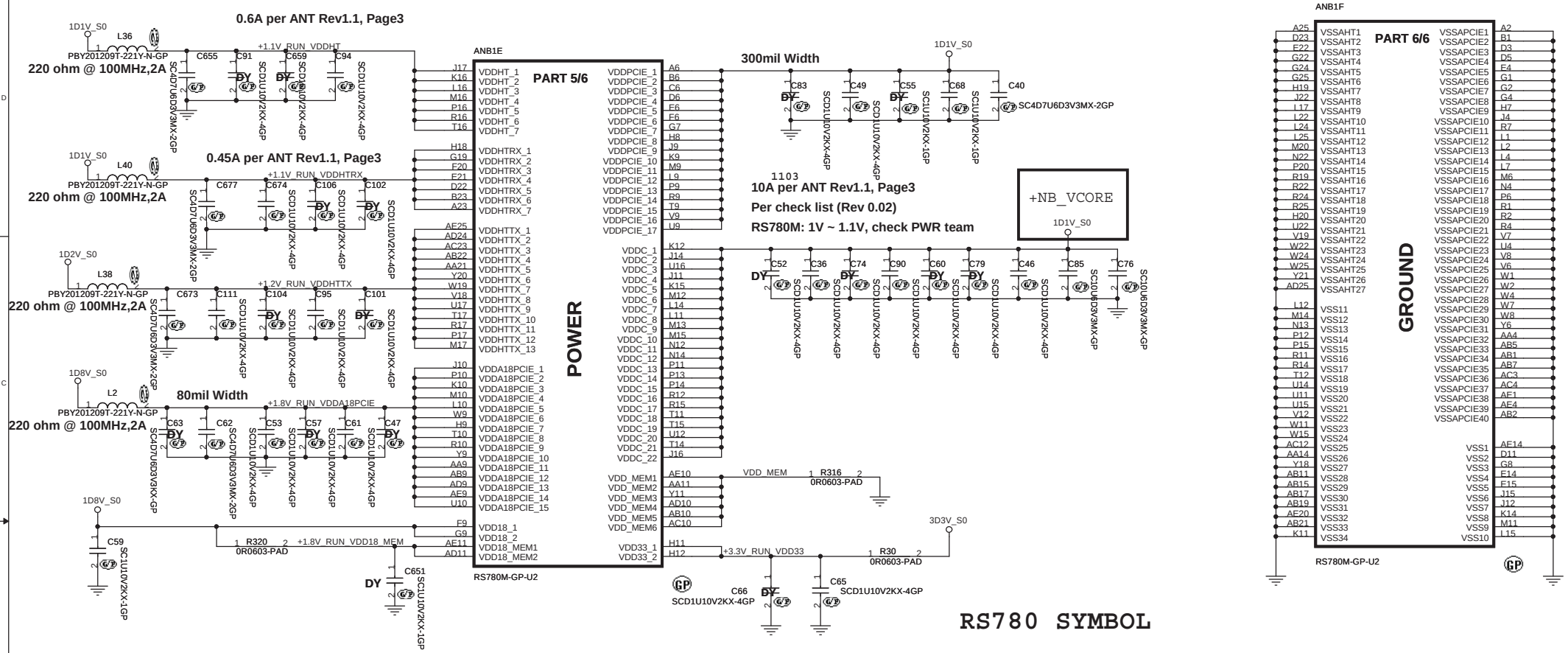
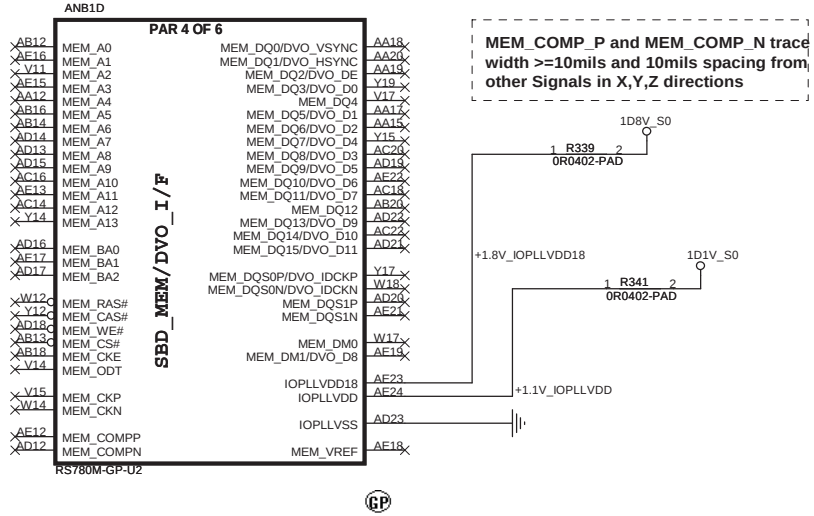
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	CPU_Power_(4/4)	
Size A3	Document Number JV71-TR	Rev SA
Date: Monday, July 06, 2009	Sheet 7 of 61	


ANB1A
PART 1 OF 6
HYPER TRANSPORT CPU I/F
RS780 SYMBOL
Placement: close RS780
Place < 100mils from pin C23 and A24
Place < 100mils from pin B25 and B24
RS780M-GP-U2
ANB1B
PART 2 OF 6
PCIE I/F GFX
PCIE I/F GPP
PCIE I/F SB
for TR
LAN
MINICARD1
A-LINK
Place < 100mils from pin AC8 and AB8
RS780M-GP-U2
RS780M Display Port Support(muxed on GFX)
DP0 GFX_TX0,TX1,TX2,TX3,AUX0,HPD0
DP1 GFX_TX4,TX5,TX6,TX7,AUX1,HPD1
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
ATi-RS880M_HT LINK&PCIe(1/3)
Size A3
Document Number
JV71-TR
Rev SA
Date: Monday, July 06, 2009
Sheet 8 of 61


Reserve for EMI 0408
EC962 SC1KP50V2KX-1GP
STRAP_DEBUG_BUS_GPIO_ENABLEb
Enables the Test Debug Bus using GPIO.(PIN: RS780M--> VSYNC#)
*1 :Disable 0 : Enable
RS780: Enables Side port memory (RS780 use HSYNC#)
*1 :Disable 0 : Enable
SUS_STAT#
Selects Loading of STRAPS From EEPROM
*1 : Bypass the loading of EEPROM straps and use Hardware Default Values
0 : I2C Master can load strap values from EEPROM if connected, or use default values if not connected
Close to NB ball
2009/04/22 R609 Change to 1K By John
for TR
2009/05/26 SB Change
80.10715.L04
2ND = 77.C1071.081
3RD = 77.21071.09L
ENABLE External CLK GEN
ANB1C
PART 3 OF 6
CRT/TVOUT
PWR
LVTM
PLL
CLOCKs
PM
MIS.
RS780M-GP-U2
RS780 SYMBOL
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title
ATi-RS880M LVDS&CRT (2/3)
Size A3
Document Number JV71-TR
Rev SA
Date: Monday, July 06, 2009
Sheet 9 of 61





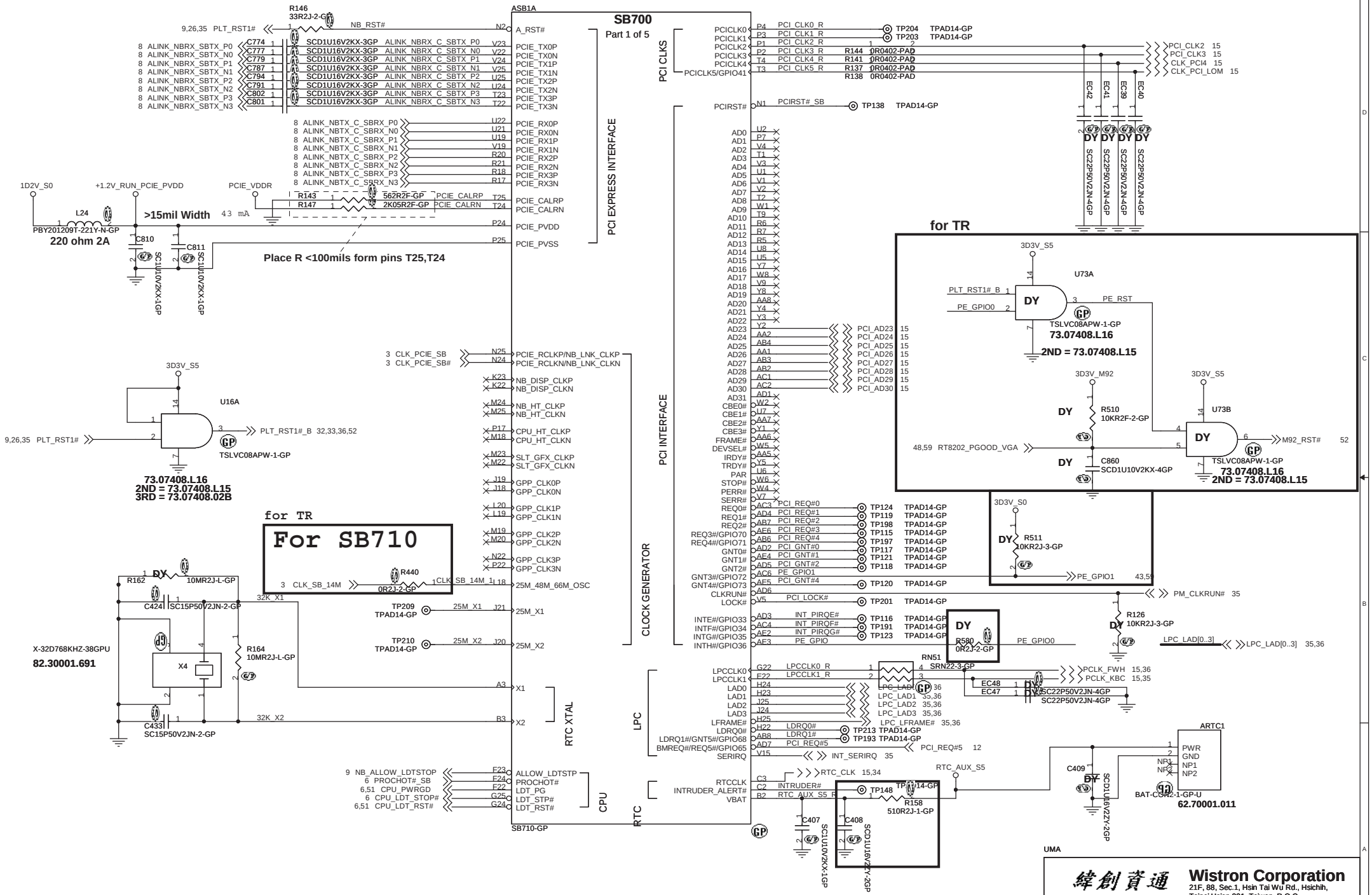
UMA

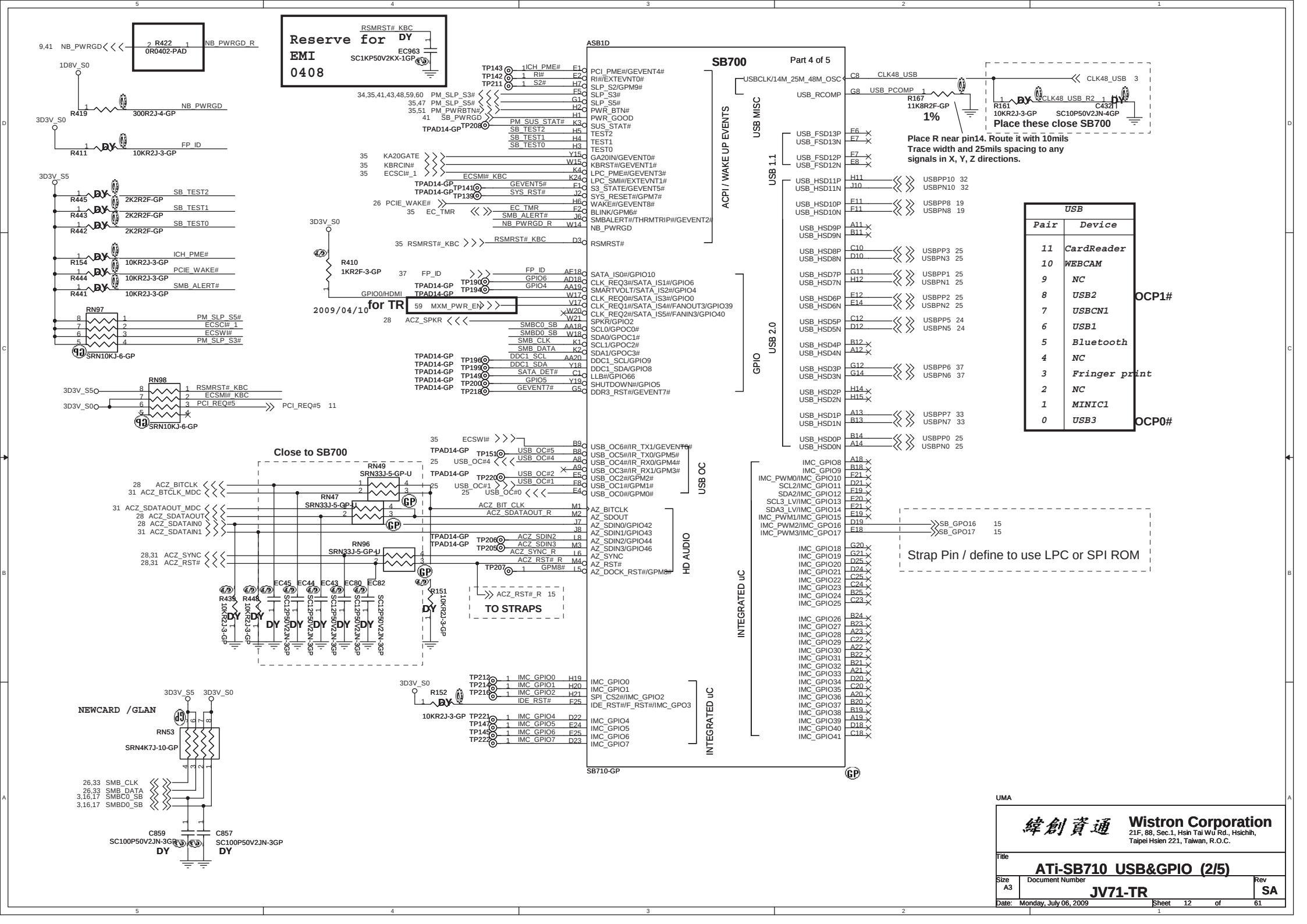
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

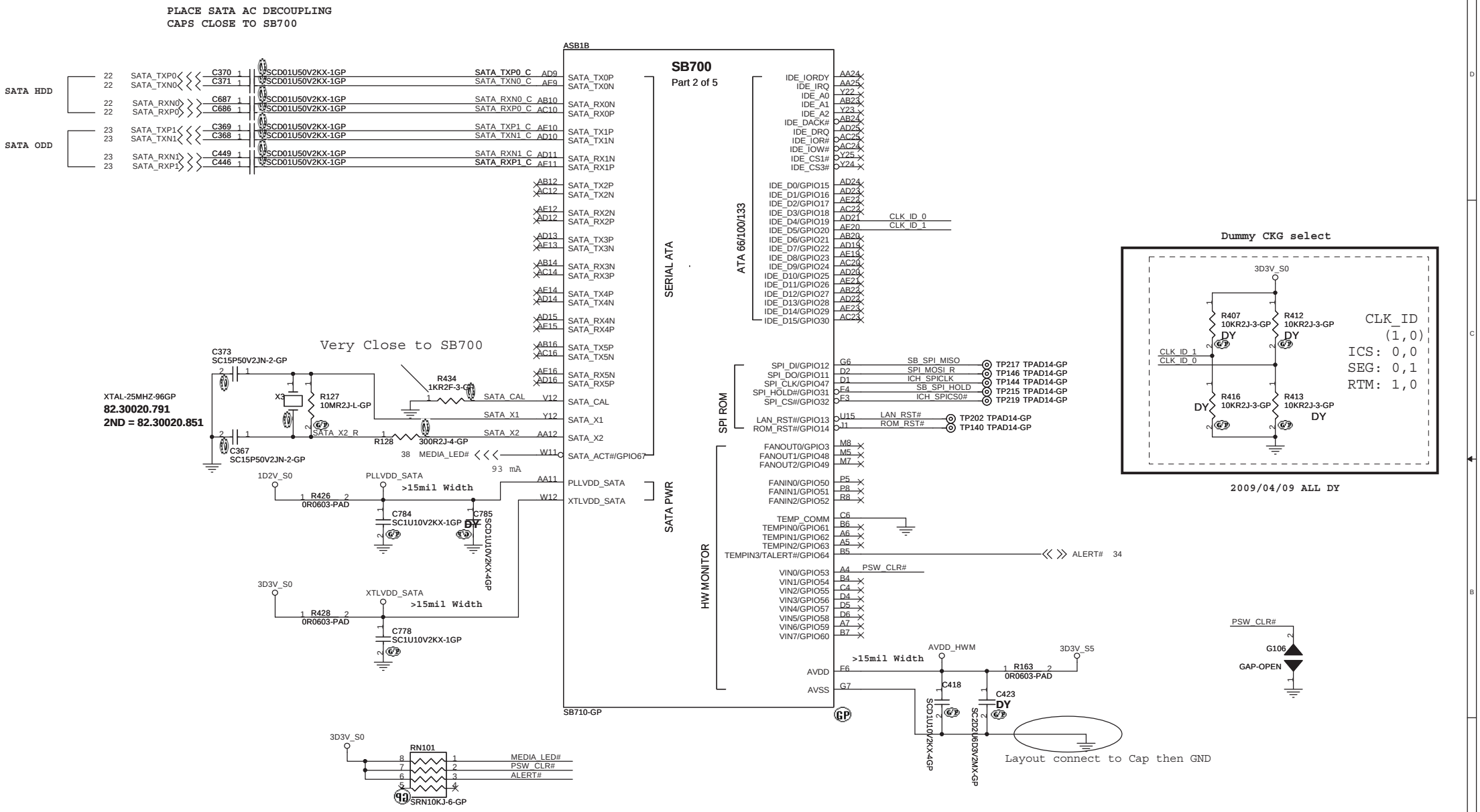
Title: **ATi-RS880M Side Port&PWR&GND(3/3)**

Size	Document Number	Rev
A3	JV71-TR	SA

Date: Monday, July 06, 2009 Sheet 10 of 61

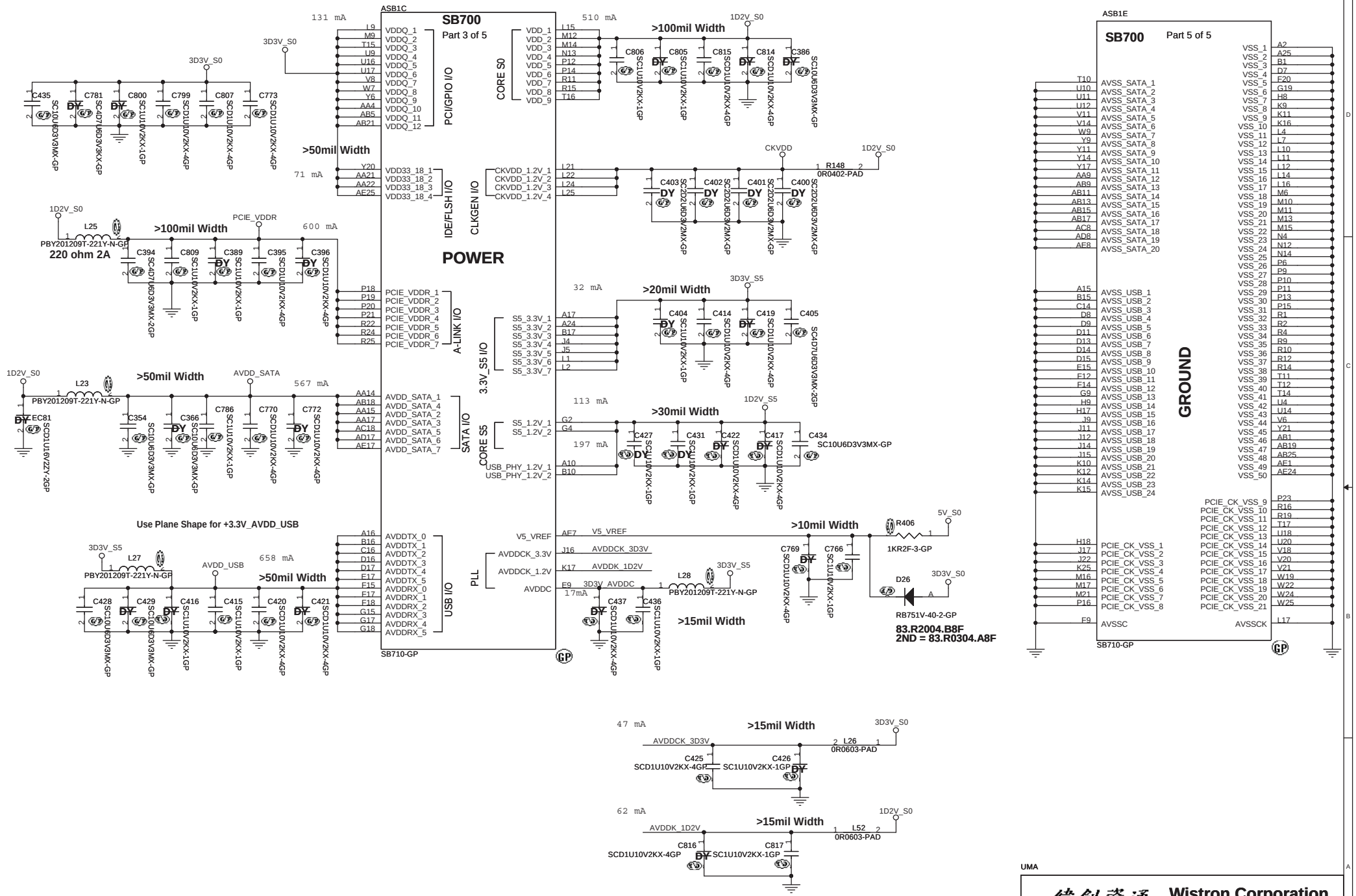

SB700
Part 1 of 5
ASB1A
PCI CLKS
PCI EXPRESS INTERFACE
PCI INTERFACE
CLOCK GENERATOR
RTC XTAL
LPC
CPU
RTC
SB710-GP
>15mil Width
220 ohm 2A
Place R <100mils form pins T25,T24
for TR
For SB710
73.07408.L16
2ND = 73.07408.L15
3RD = 73.07408.02B
X-32D768KHZ-38GPU
82.30001.691
ARTC1
BAT-CR2-1-GP-U
62.70001.011
UMA
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
ATi-SB710 PCIE&PCI (1/5)
Size A3
Document Number
JV71-TR
Rev SA
Date: Monday, July 06, 2009
Sheet 11 of 61


Reserve for EMI 0408
SB700
Part 4 of 5
ASB1D
SB710-GP
Place these close SB700
Place R near pin14. Route it with 10mils Trace width and 25mils spacing to any signals in X, Y, Z directions.
Close to SB700
Strap Pin / define to use LPC or SPI ROM
TO STRAPS
NEWCARD /GLAN
USB
Pair Device
11 CardReader
10 WEBCAM
9 NC
8 USB2 OCP1#
7 USBCN1
6 USB1
5 Bluetooth
4 NC
3 Fringer print
2 NC
1 MINIC1
0 USB3 OCP0#
2009/04/10 for TR
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
ATi-SB710 USB&GPIO (2/5)
JV71-TR
SA
Date: Monday, July 06, 2009
Sheet 12 of 61



UMA

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	**ATi-SB710 SATA-IDE (3/5)**
Size: A3	Document Number: **JV71-TR**
Rev: SB	
Date: Monday, July 06, 2009	Sheet 13 of 61



UMA

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

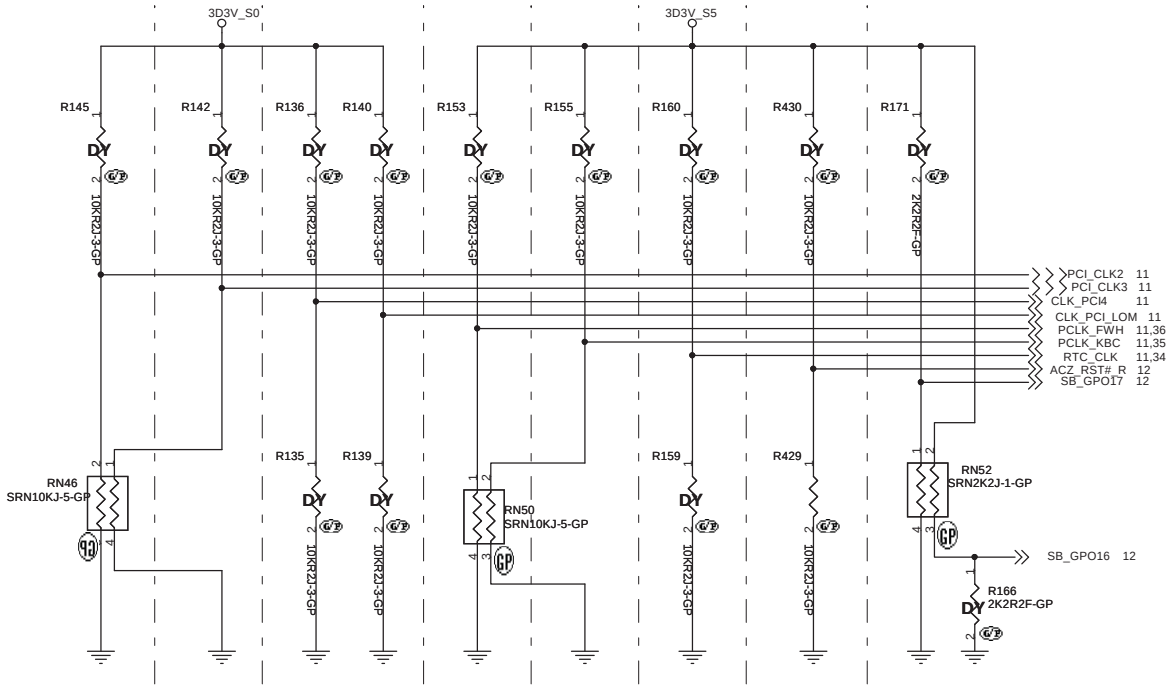
Title: **ATi-SB710 POWER&GND (4/5)**

Size	Document Number	Rev
A3	JV71-TR	SB

Date: Monday, July 06, 2009 Sheet 14 of 61

REQUIRED STRAPS

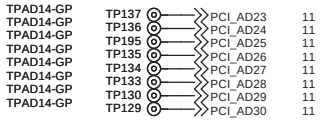
REQUIRED SYSTEM STRAPS



	PCI_CLK2	PCI_CLK3	CLK_PCI_LOM CLK_PCI4	PCLK_FWH	PCLK_KBC	RTCCLK	AZ_RST#	SB_GPO17 , SB_GPO16
PULL HIGH	WatchDOG (NB_PWRGD) ENABLED	USE DEBUG STRAPS	RESERVED	IMC ENABLED	CLKGEN ENABLED (Use Internal)	INTERNAL RTC DEFAULT	ENABLE PCI ROM BOOT	ROM TYPE: H, H = Reserved H, L = SPI ROM L, H = LPC ROM DEFAULT L, L = FWH ROM
PULL LOW	WatchDog (NB_PWRGD) DISABLED DEFAULT	IGNORE DEBUG STRAPS DEFAULT		IMC DISABLED DEFAULT	CLKGEN DISABLED (Use External) DEFAULT	EXT. RTC (PD on X1, apply 32KHz to RTC_CLK)	DISABLE PCI ROM BOOT DEFAULT	

NOTE: SB700 HAS INTERNAL 15K PULL UP RESISTOR FOR RTCCLK

DEBUG STRAPS



	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23	PCI_AD30 PCI_AD29
PULL HIGH	USE LONG RESET (DEFAULT)	USE PCI PLL (DEFAULT)	USE ACPI BCLK (DEFAULT)	USE IDE PLL (DEFAULT)	USE DEFAULT PCIE STRAPS (DEFAULT)	Reserved (DEFAULT)	Reserved
PULL LOW	USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	Reserved	

Note: SB700 has 15K internal PU FOR PCI_AD[30:23]

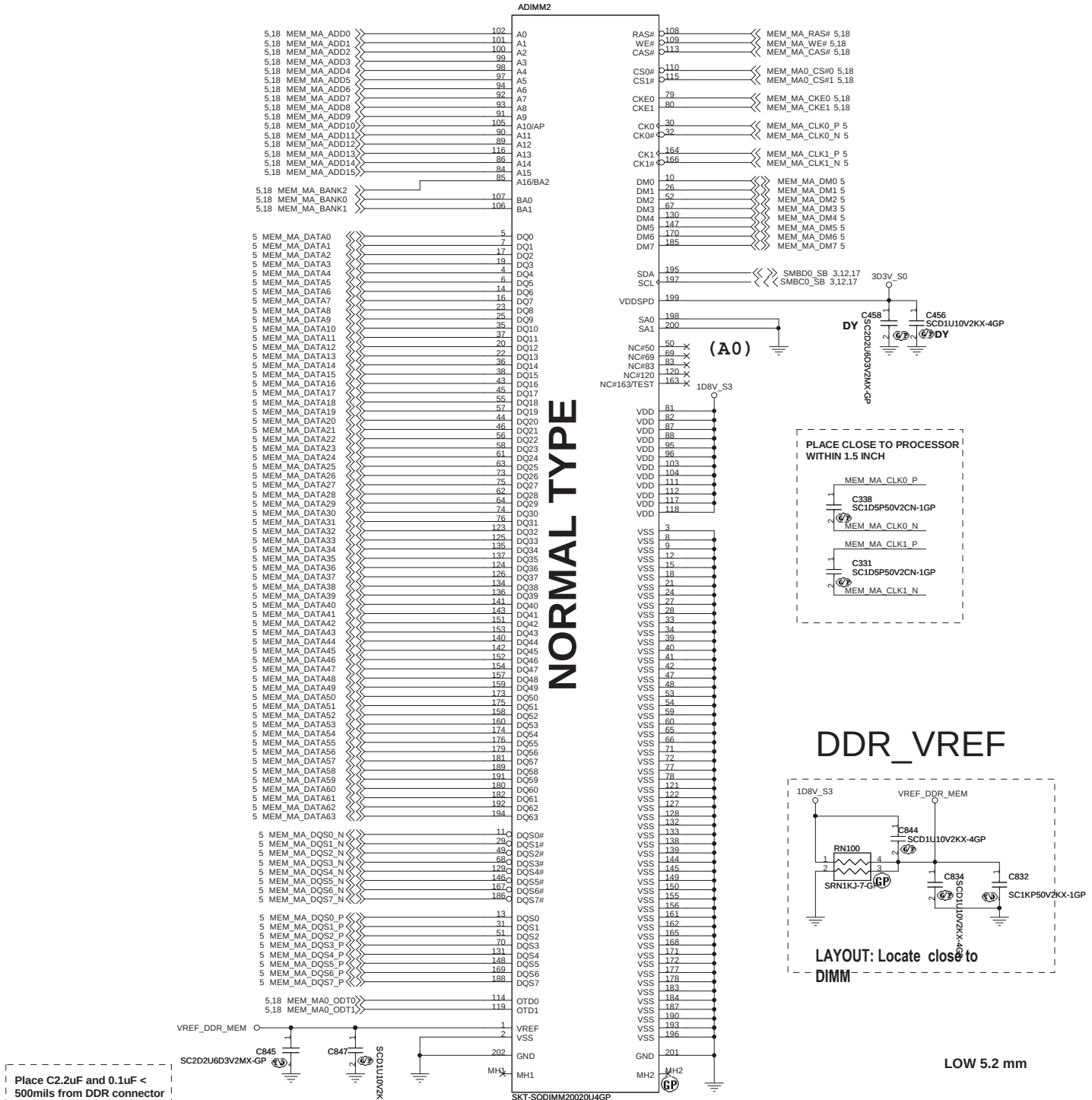
UMA

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ATi-SB710 STRAPPING (5/5)

Size: A3 | Document Number: JV71-TR | Rev: SA

Date: Monday, July 06, 2009 | Sheet 15 of 61



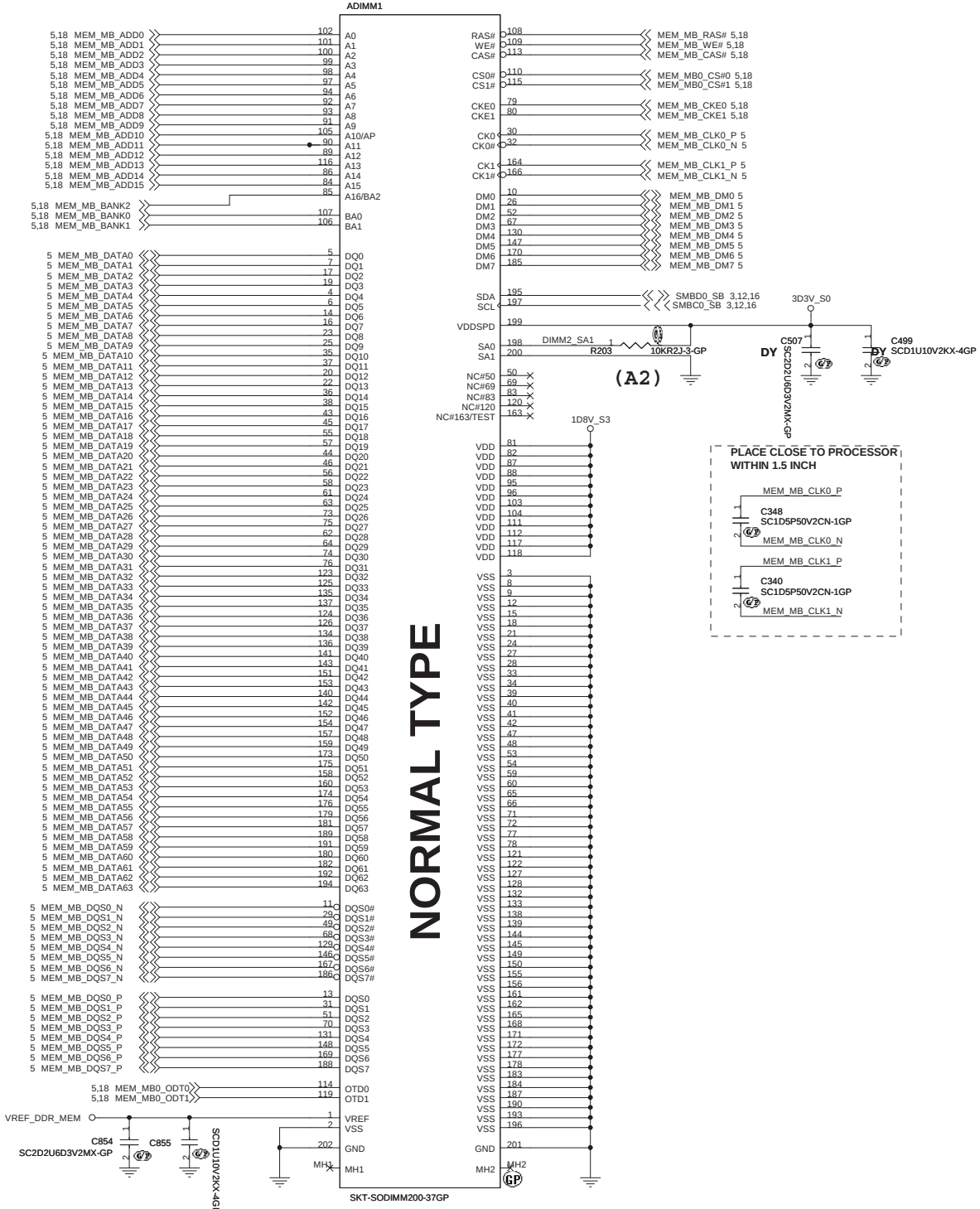
UMA

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **DDR_SO-DIMM SKT_1**

Size	Document Number	Rev
Custom	JV71-TR	SB

Date: Monday, July 06, 2009 Sheet 16 of 61



62.10017.E21
2ND = 62.10017.A51
3RD = 62.10017.G71

HI 9.2mm

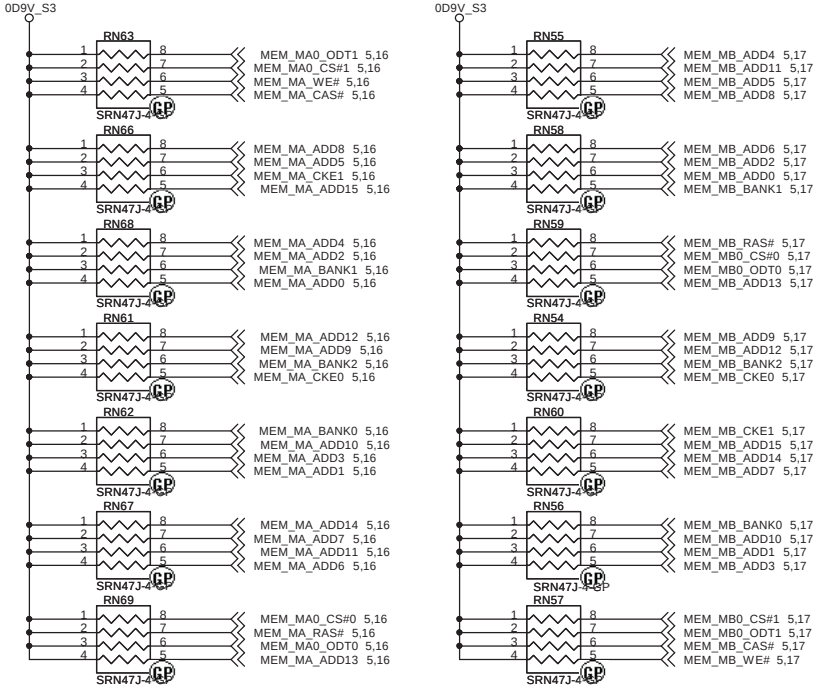
UMA

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title	DDR SO-DIMM SKT_2	
Size: Custom	Document Number: JV71-TR	Rev: SB
Date: Monday, July 06, 2009	Sheet 17 of 61	

PARALLEL TERMINATION

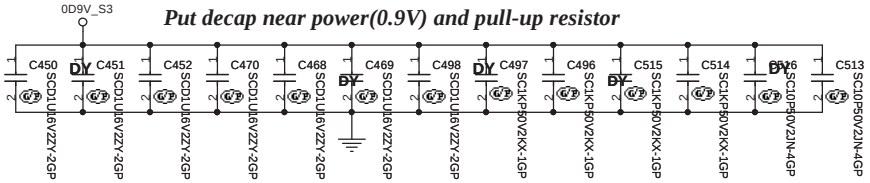
Put decap near power(0.9V) and pull-up resistor



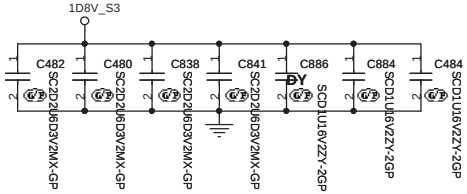
Do not share the Term resistor between the DDR addess and Control Signals.

Decoupling Capacitor

Put decap near power(0.9V) and pull-up resistor

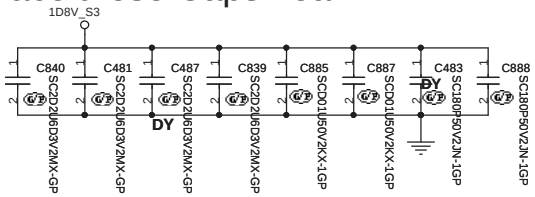


Place these Caps near DM1



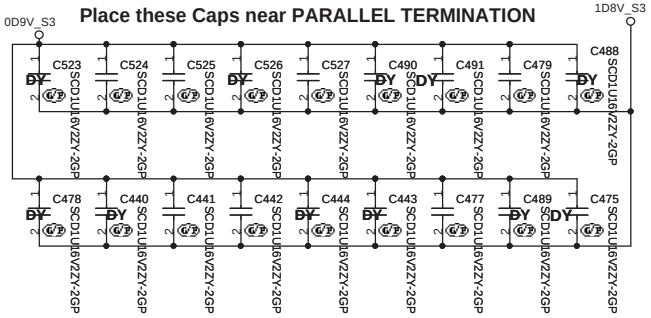
Layout Note:
Place one cap close to every 2 pullup resistors terminated to 0D9V_S3

Place these Caps near DM2



Layout Note:
Place one cap close to every 2 pullup resistors terminated to 0D9V_S3

Place these Caps near PARALLEL TERMINATION

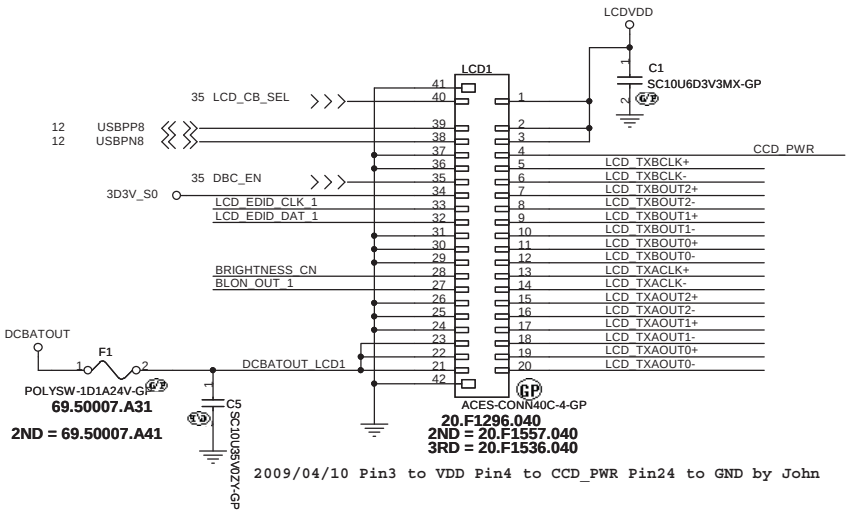


UMA

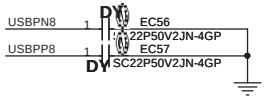
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

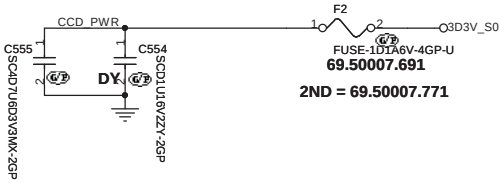
Title	**DDR_DAMPING & TERMINATION**	
Size A3	Document Number **JV71-TR**	Rev **SB**
Date: Monday, July 06, 2009	Sheet 18 of 61	

LCD/INVERTER/CCD CONN

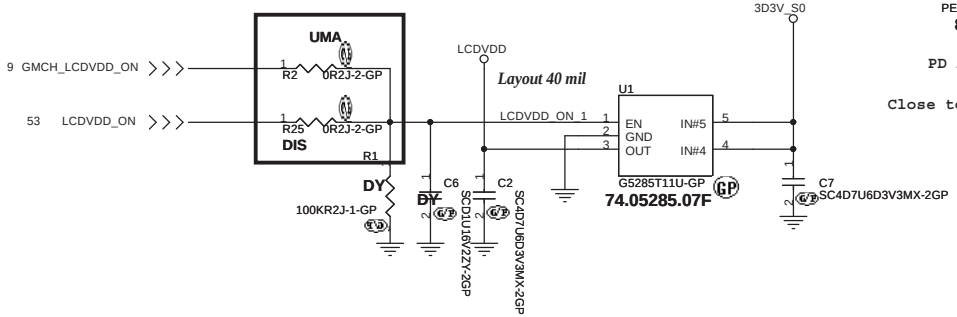


2009/04/10 Pin3 to VDD Pin4 to CCD_PWR Pin24 to GND by John

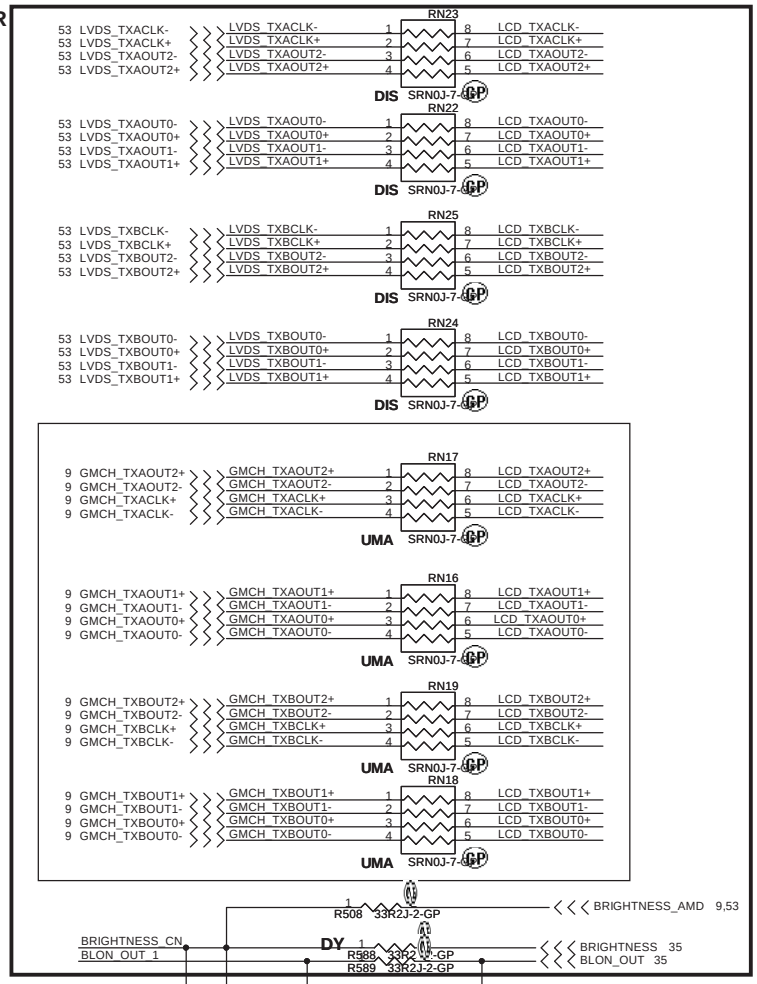




for TR



for TR



Inverter Pin	
Pin	Symbol
1	Vin
2	Vin
3	Brightness
4	BLON
5	GND
6	GND

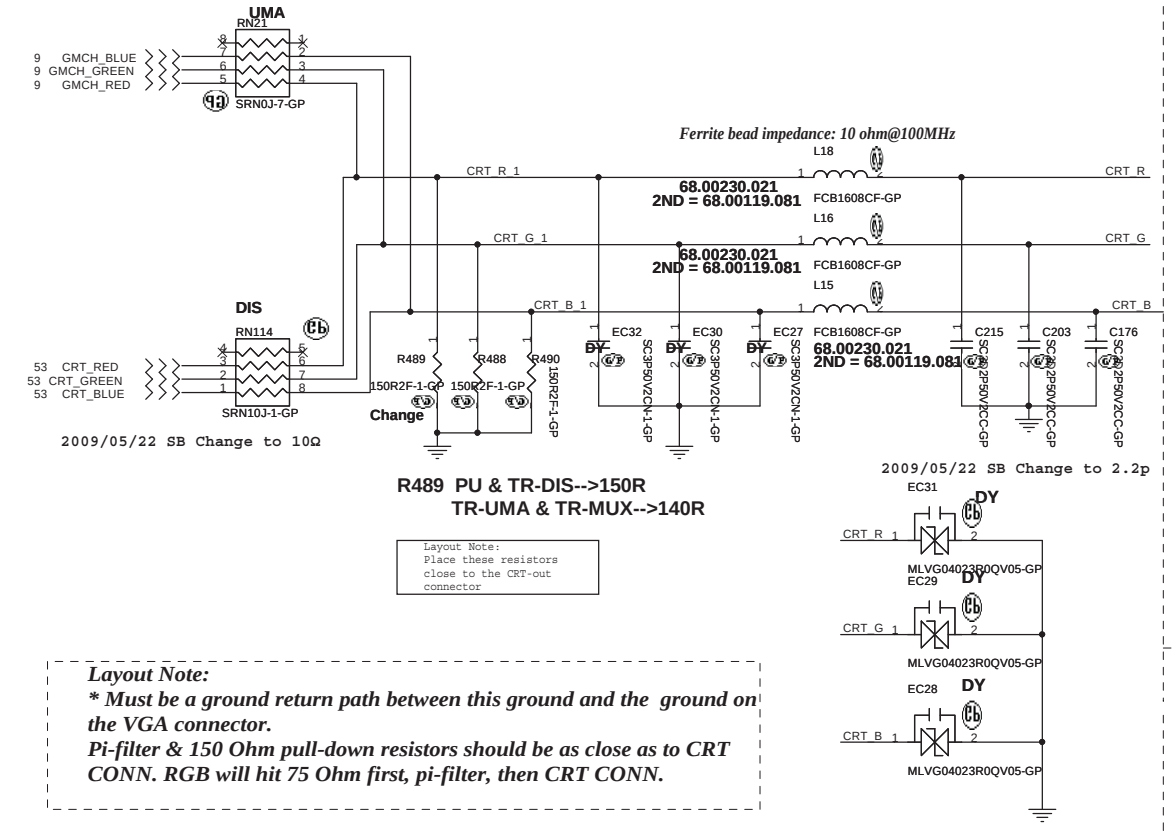
CCD Pin	
Pin	Symbol
1	CCD_PWR
2	USB-
3	USB+
4	GND
5	GND

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: LCD CONN

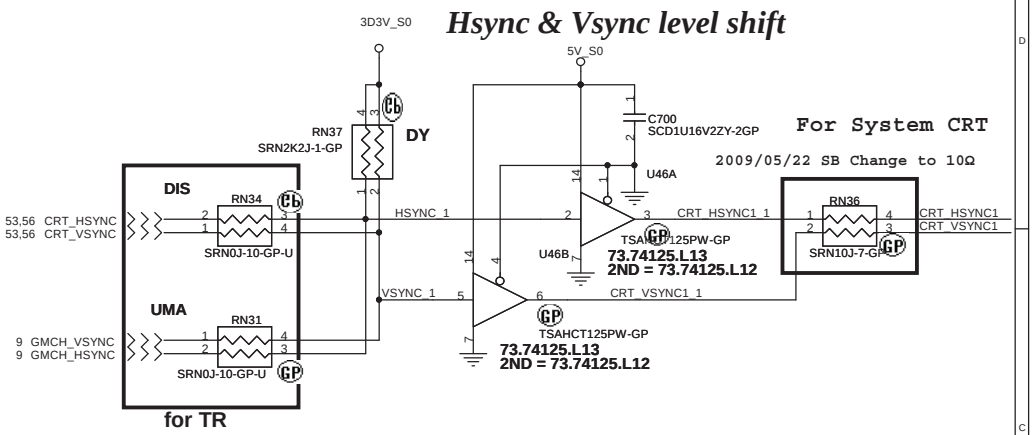
Size: A3 | Document Number: JV71-TR | Rev: -1

Date: Monday, July 06, 2009 | Sheet 19 of 61

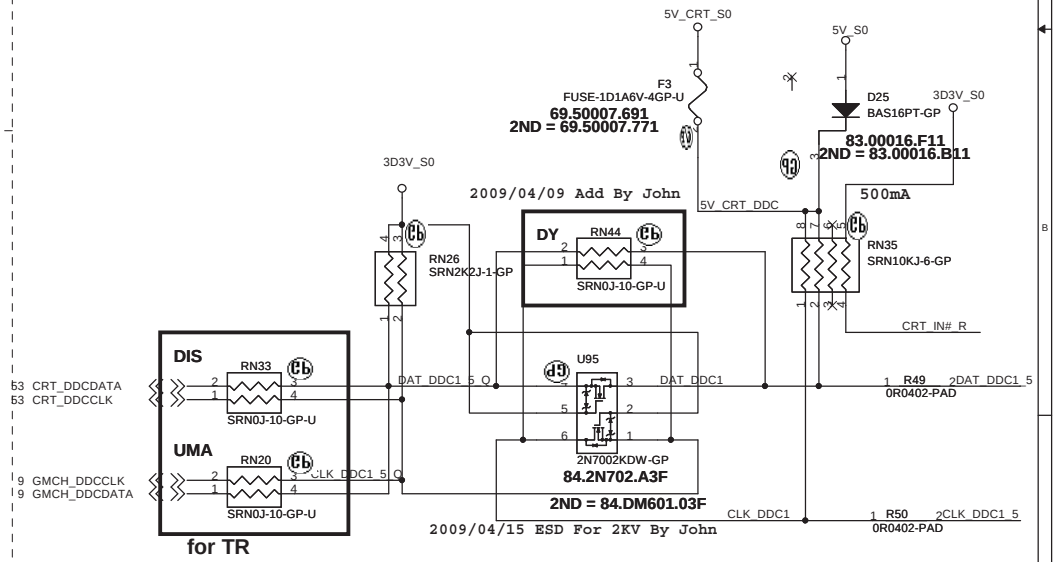


Layout Note:
** Must be a ground return path between this ground and the ground on the VGA connector.*
Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN. RGB will hit 75 Ohm first, pi-filter, then CRT CONN.

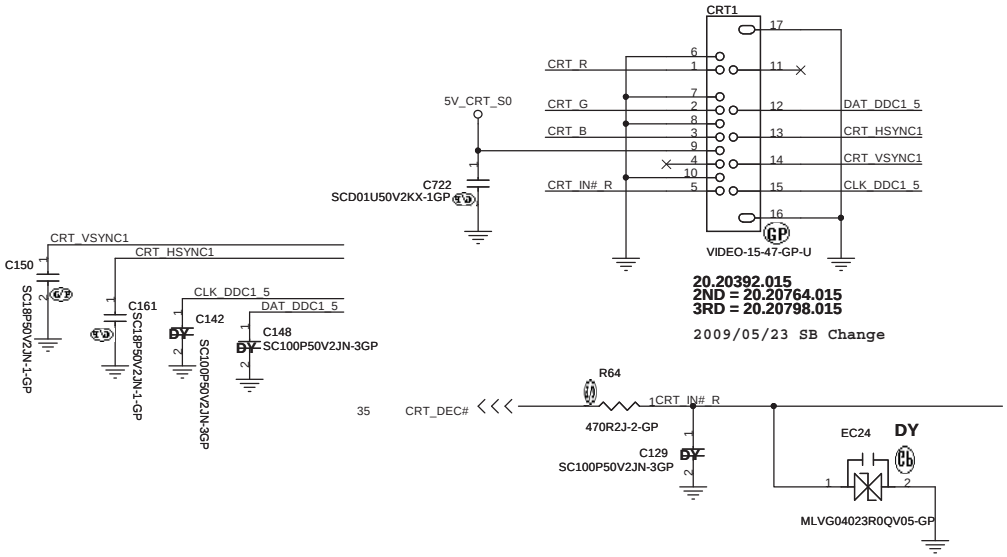
Hsync & Vsync level shift



DDC_CLK & DATA level shift

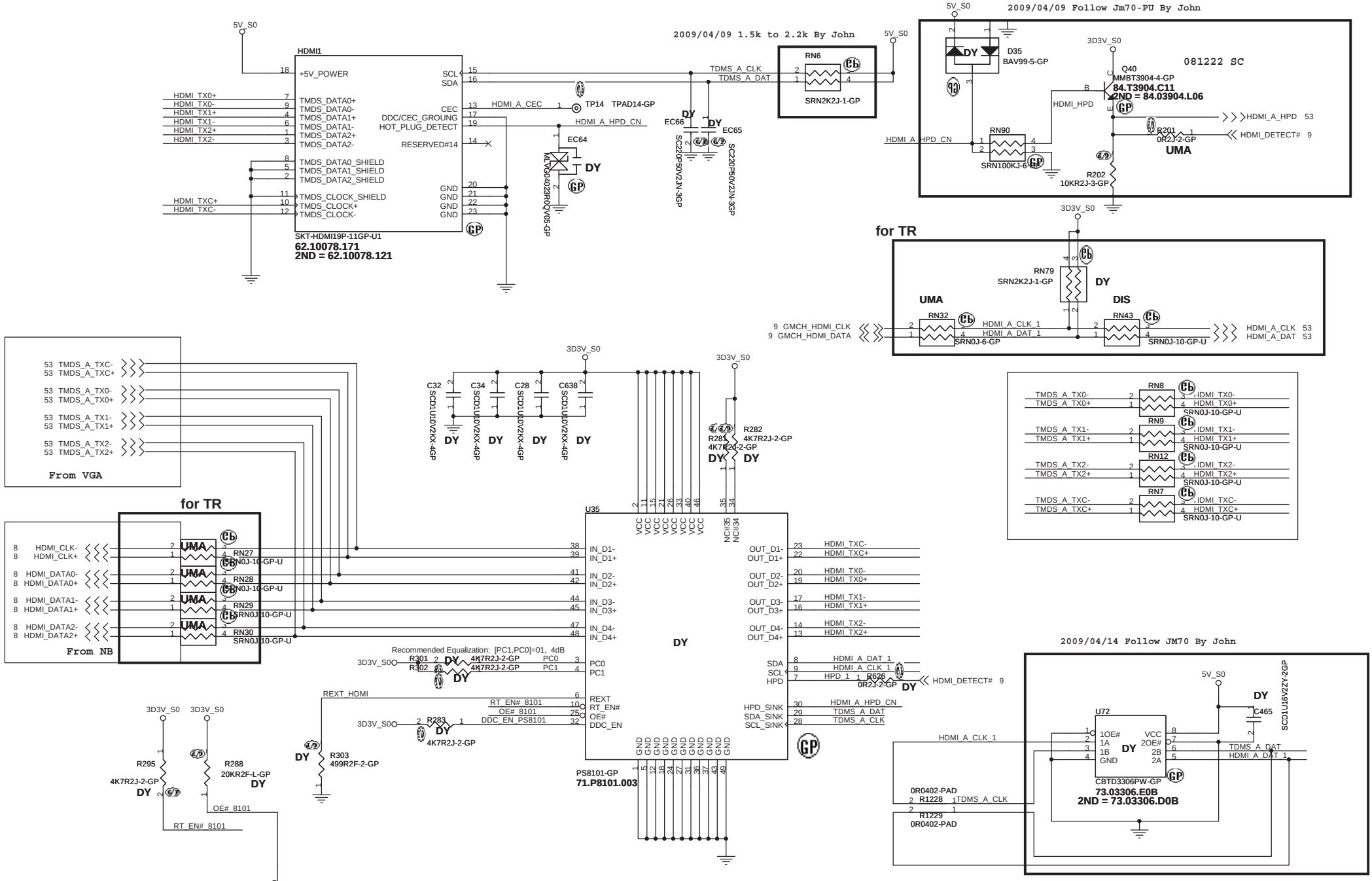


CRT I/F & CONNECTOR

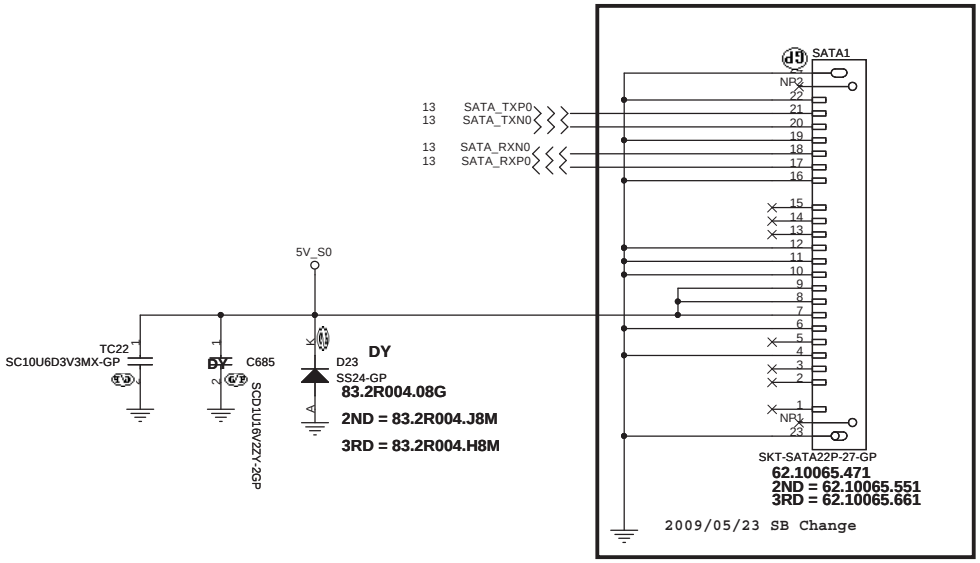


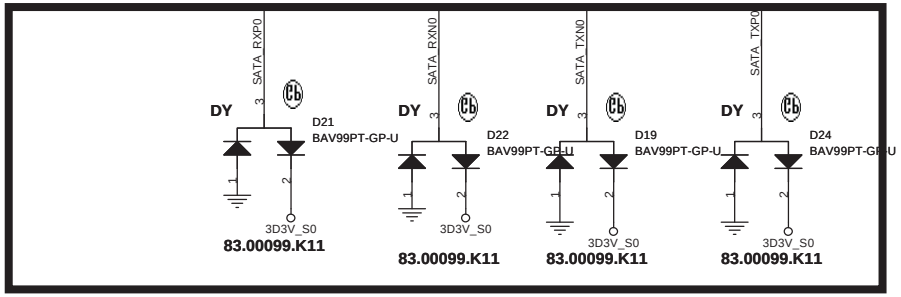
UMA

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	**CRT Connector**
Size / Document Number	**JV71-TR**
Rev	**SB**
Date: Monday, July 06, 2009	Sheet 20 of 61


2009/04/09 Follow Jm70-PU By John
2009/04/09 1.5k to 2.2k By John
HDMI1
SKT-HDMI19P-11GP-U1
62.10078.171
2ND = 62.10078.121
RN6
SRN2K2J-1-GP
D35
BAV99-5-GP
Q40
MMBT3904-4-GP
84.T3904.C11
2ND = 84.03904.L06
081222 SC
RN90
SRN100KJ-6-GP
R201
0R2J-2-GP
R202
10KR2J-3-GP
UMA
for TR
RN79
SRN2K2J-1-GP
DIS
RN32
SRN0J-6-GP
RN43
SRN0J-10-GP-U
RN8
RN9
RN12
RN7
From VGA
From NB
U35
PS8101-GP
71.P8101.003
2009/04/14 Follow JM70 By John
U72
CBTD3306PW-GP
73.03306.E0B
2ND = 73.03306.D0B
Q19
2N7002E-1-GP
84.2N702.D31
2ND = 84.2N702.E31
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
HDMI Connector
Size
Document Number
JV71-TR
Rev
SB
Date: Monday, July 06, 2009
Sheet 21 of 61

SATA Connector

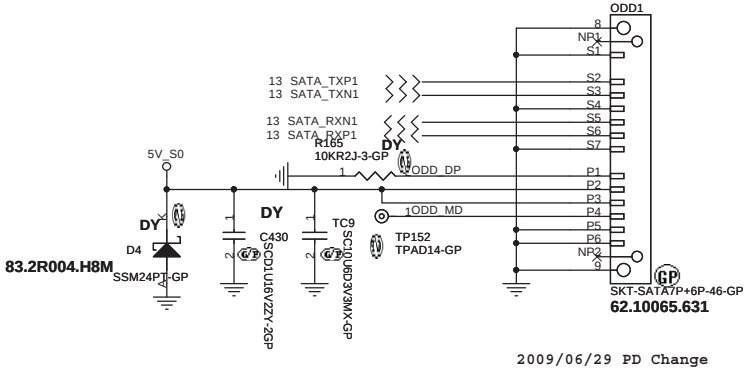


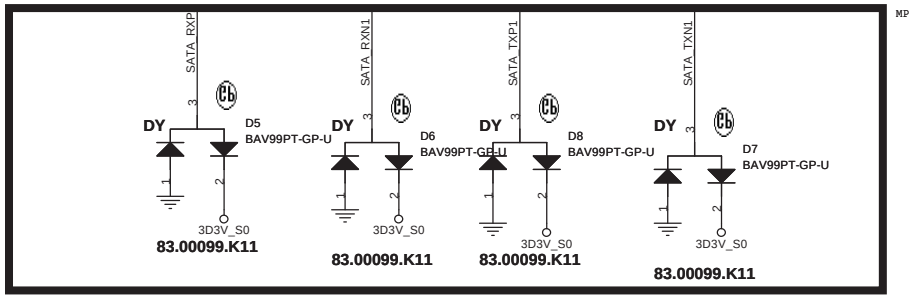


UMA

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	**HDD**	
Size	Document Number **JV71-TR**	Rev **SB**
Date: Monday, July 06, 2009	Sheet 22 of 61	

SATA ODD Connector



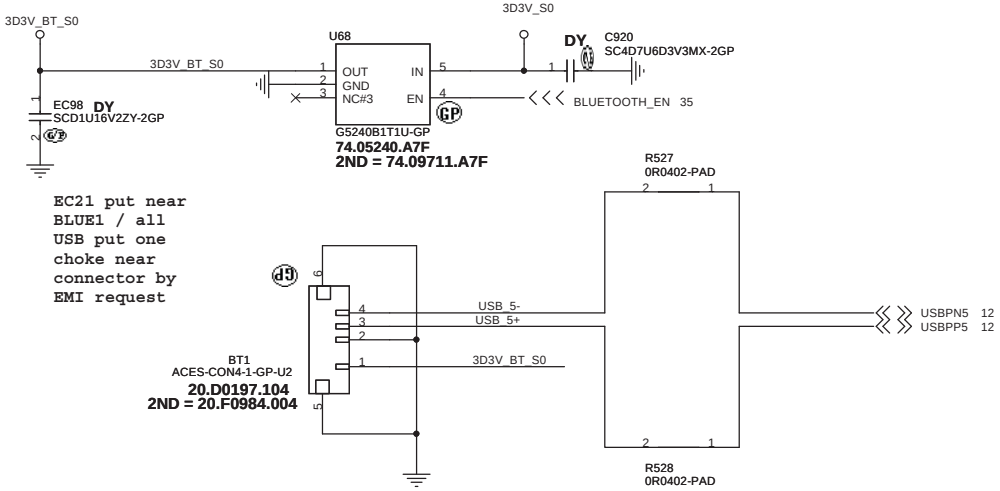


UMA

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	**ODD**	
Size	Document Number **JV71-TR**	Rev **SB**
Date: Monday, July 06, 2009	Sheet 23 of 61	

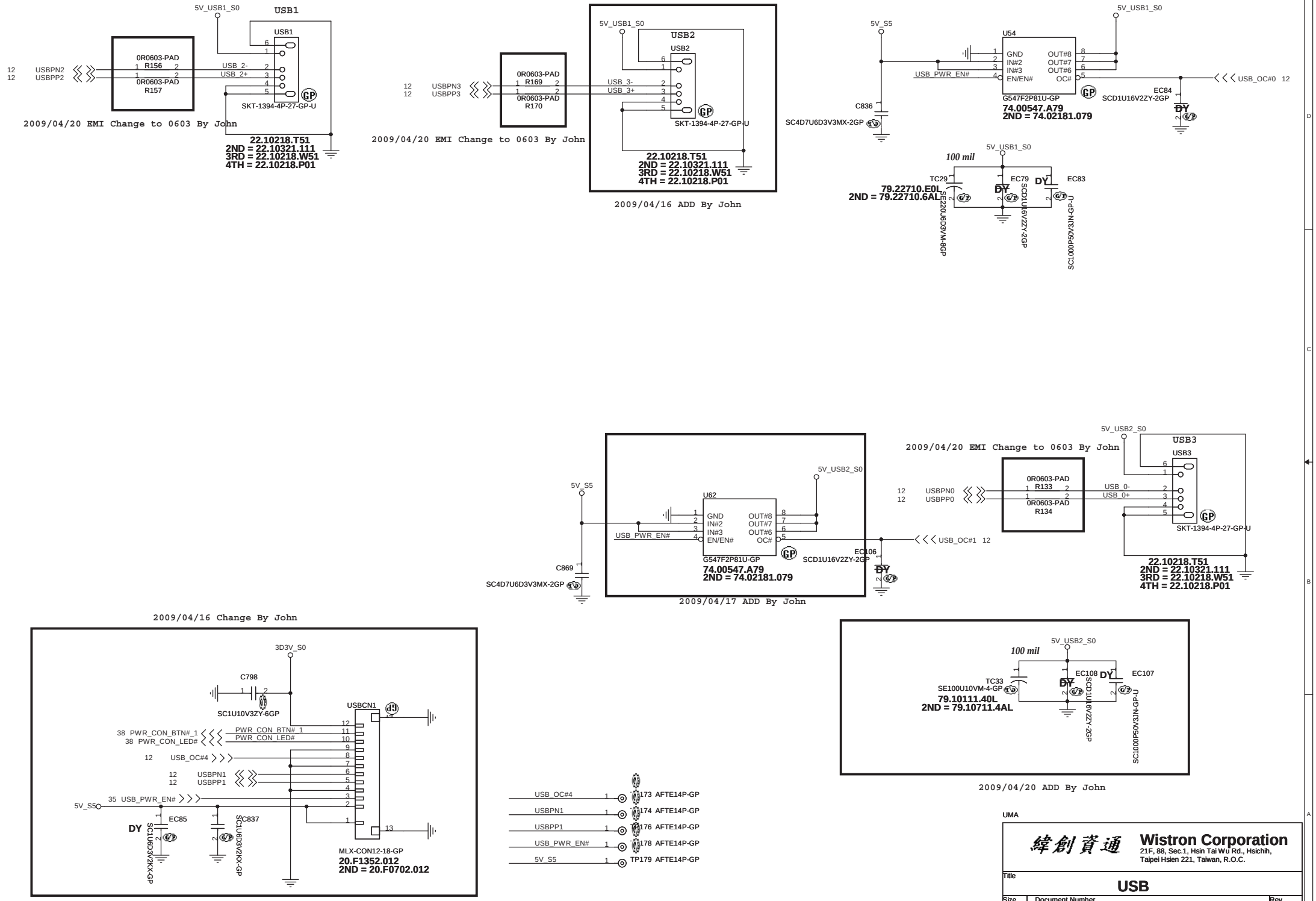
BLUETOOTH MODULE

1.5A / High Active Voltage 2V



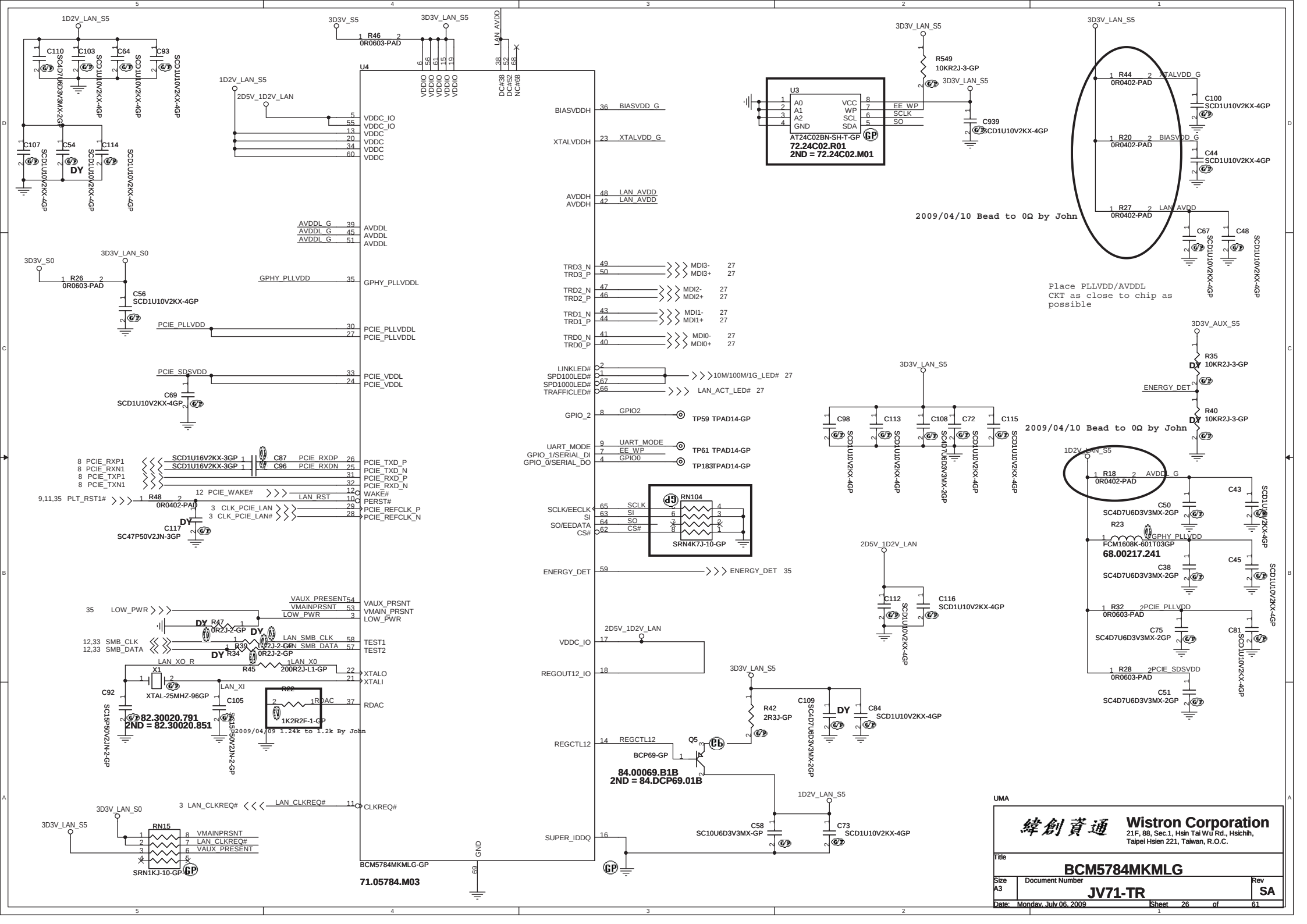
UMA

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	**BLUETOOTH**
Size / Document Number	**JV71-TR**
Rev	**SA**
Date: Monday, July 06, 2009	Sheet 24 of 61



UMA

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	**USB**	
Size	Document Number **JV71-TR**	Rev **SA**
Date: Monday, July 06, 2009	Sheet 25 of 61	


U4
BCM5784MKMLG-GP
71.05784.M03
U3
AT24C02BN-SH-T-GP
72.24C02.R01
2ND = 72.24C02.M01
2009/04/10 Bead to 0Ω by John
Place PLLVDD/AVDDL CKT as close to chip as possible
2009/04/10 Bead to 0Ω by John
68.00217.241
82.30020.791
2ND = 82.30020.851
2009/04/09 1.24k to 1.2k By John
84.00069.B1B
2ND = 84.DCP69.01B
UMA
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title
BCM5784MKMLG
Size A3
Document Number
JV71-TR
Rev SA
Date: Monday, July 06, 2009
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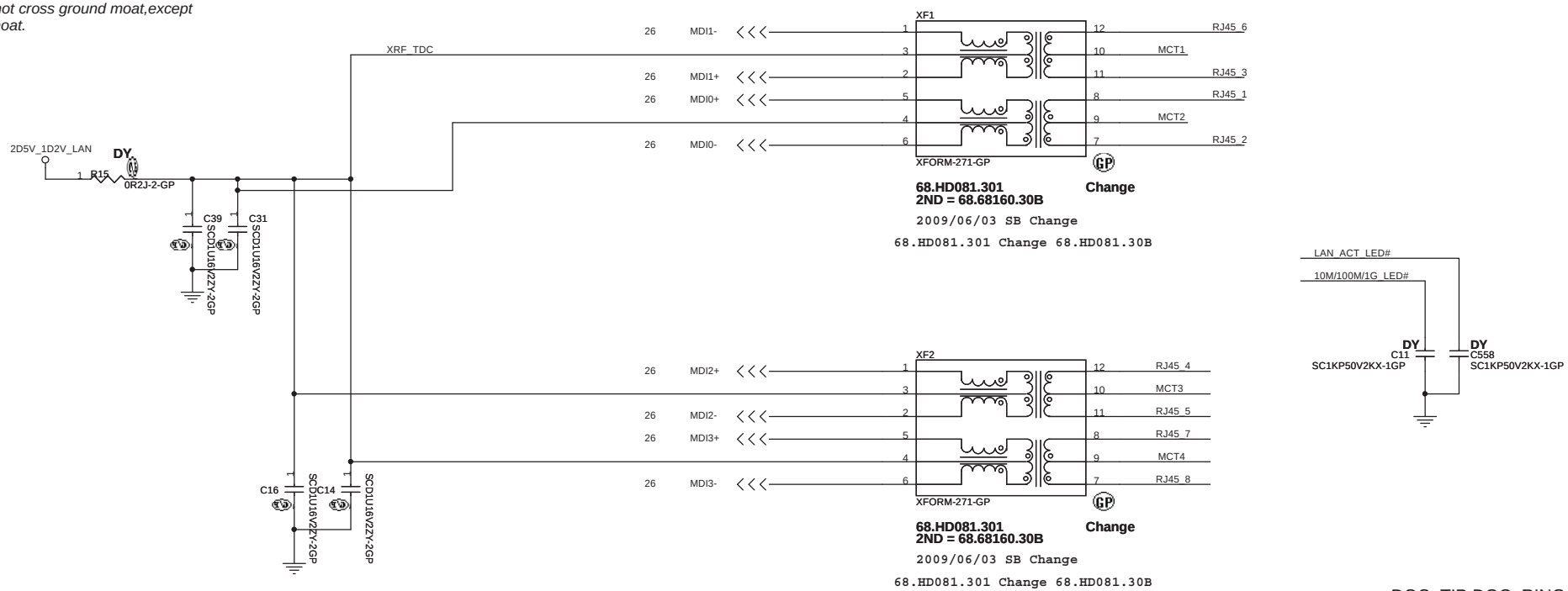
LAN Connector

GIGA Lan Transformer

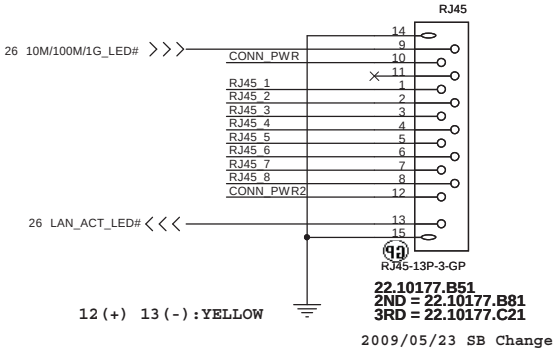
1.route on bottom as differential pairs.
2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
3.No vias, No 90 degree bends.
4.pairs must be equal lengths.
5.6mil trace width,12mil separation.
6.36mil between pairs and any other trace.
7.Must not cross ground moat,except RJ-45 moat.



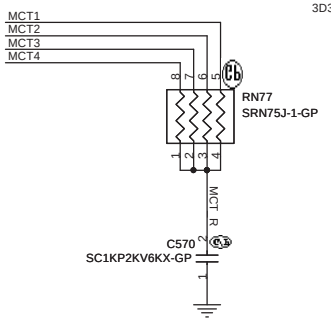
DOC_TIP,DOC_RING,TIP,RING:
W/S : 10/100 @ Surface layers
10/20 @ Inner layers

10(+) 9(-)::GREEN
10(+) 11(-):ORANGE

LAN Connector

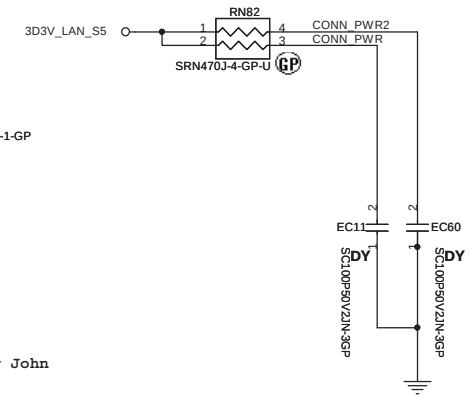


12(+) 13(-):YELLOW



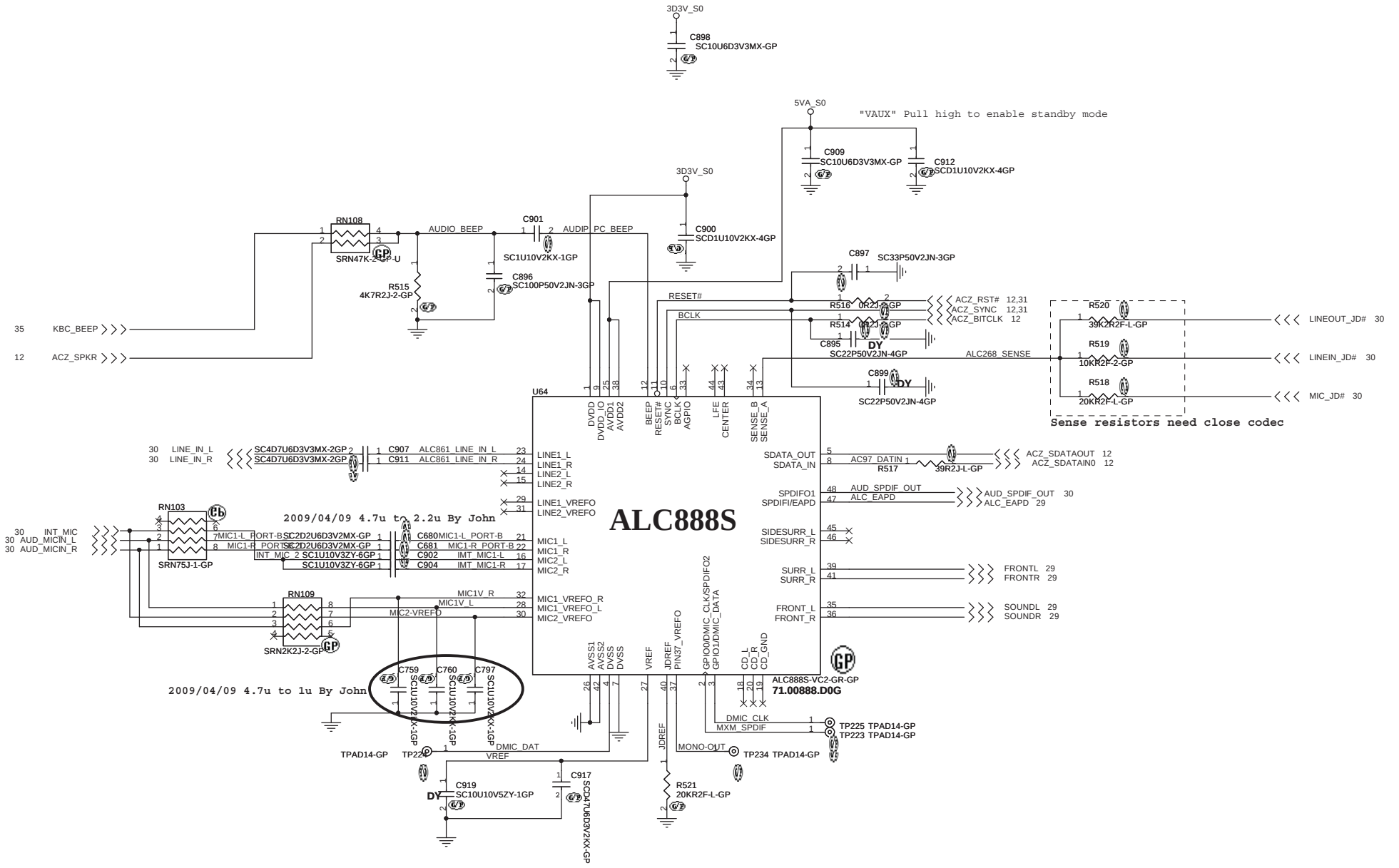
2009/04/09 Follow JV70-PU By John

2009/04/09 Change 4P2R By John



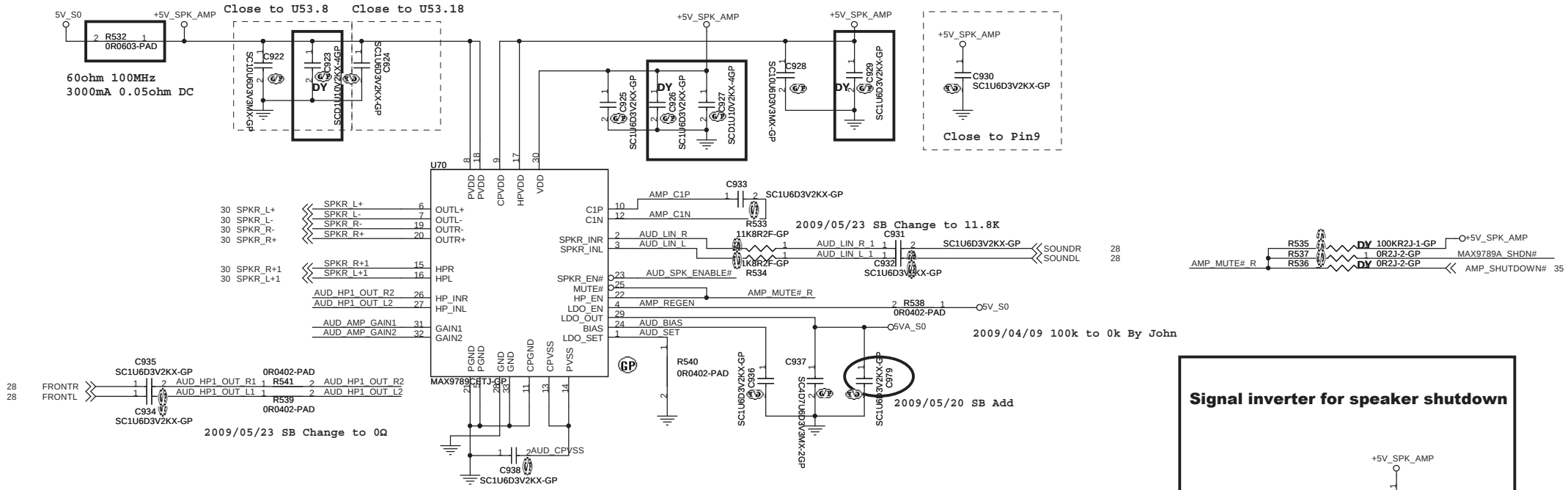
UMA

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	LAN CONN	
Size A3	Document Number JV71-TR	Rev SB
Date: Friday, July 10, 2009	Sheet 27 of 61	



UMA

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	**Azalia codec ALC888**
Size A3	Document Number **JV71-TR** Rev **SB**
Date: Monday, July 06, 2009	Sheet 28 of 61



GAIN1	GAIN2	GAIN
0	0	6dB
0	1	10dB
1	0	15.6dB
1	1	21.6dB

UMA

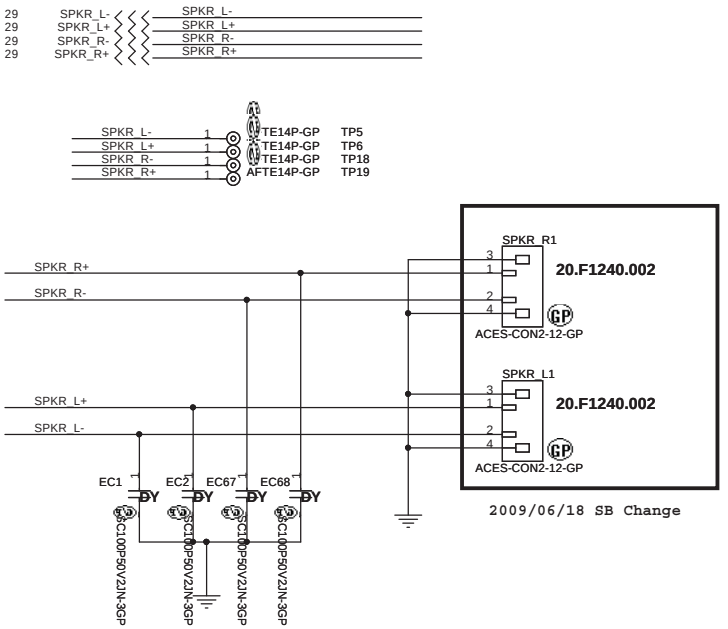
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **AUDIO AMP**

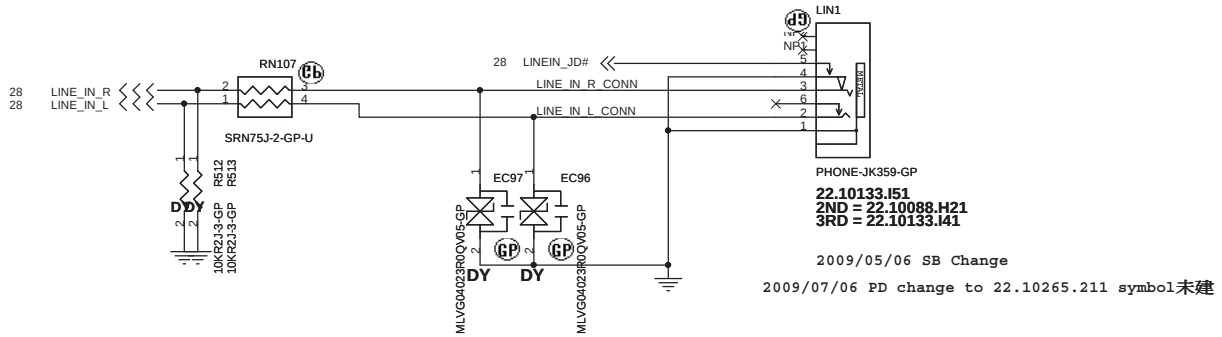
Size | Document Number: **JV71-TR** | Rev: **SB**

Date: Monday, July 06, 2009 | Sheet 29 of 61

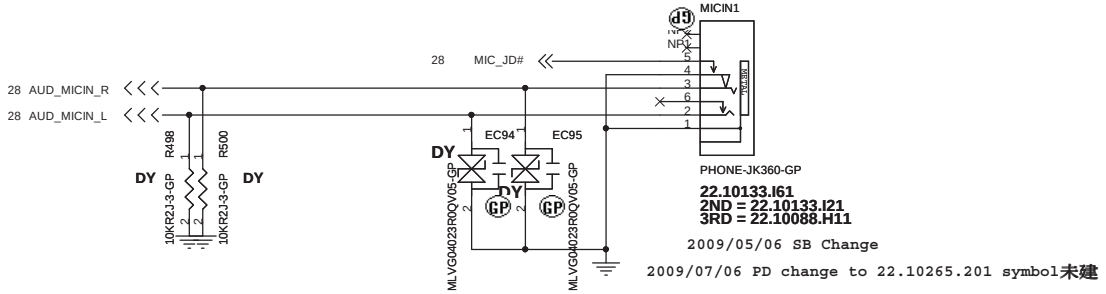
Internal Speaker



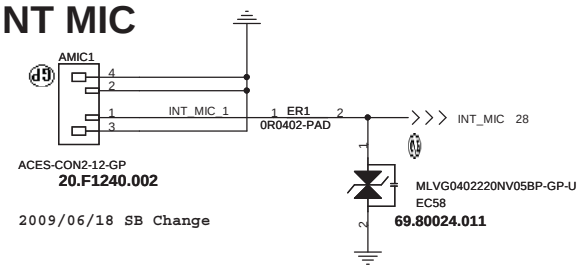
LINE IN



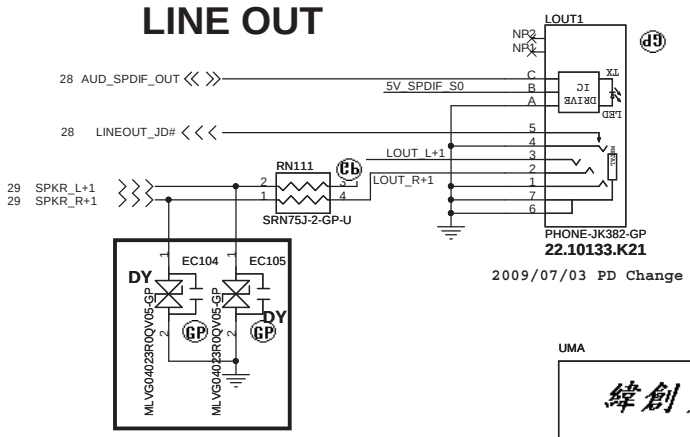
MIC IN

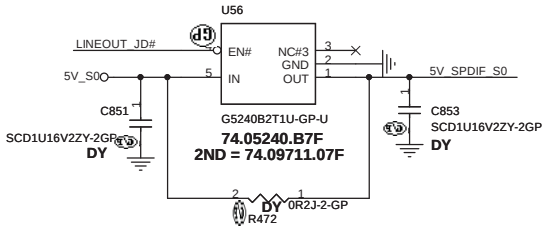


INT MIC



LINE OUT

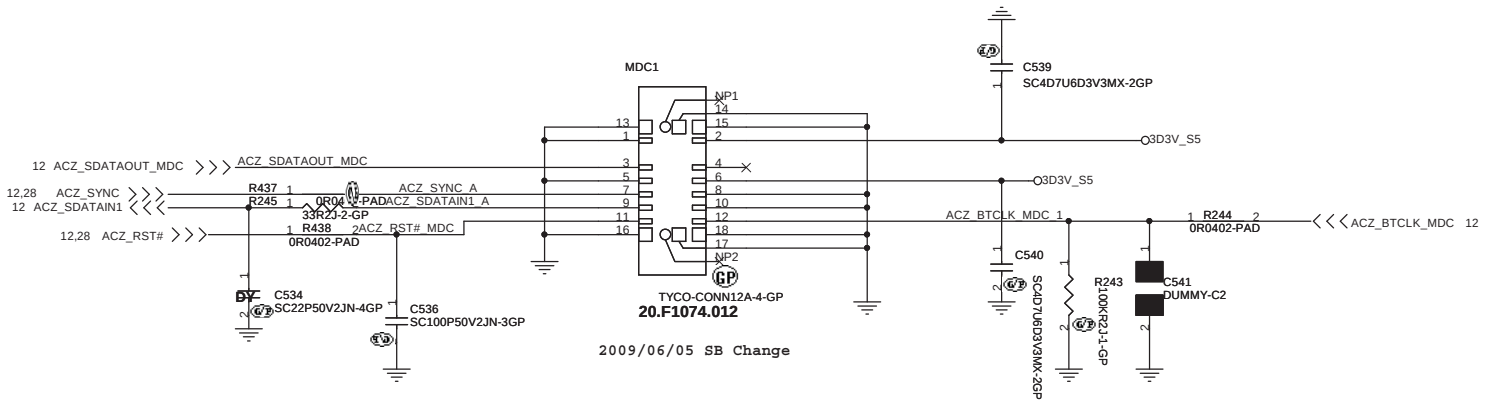


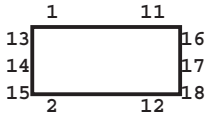


UMA

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	**AUDIO JACK**	
Size	Document Number **JV71-TR**	Rev **SB**
Date: Monday, July 06, 2009	Sheet 30 of 61	

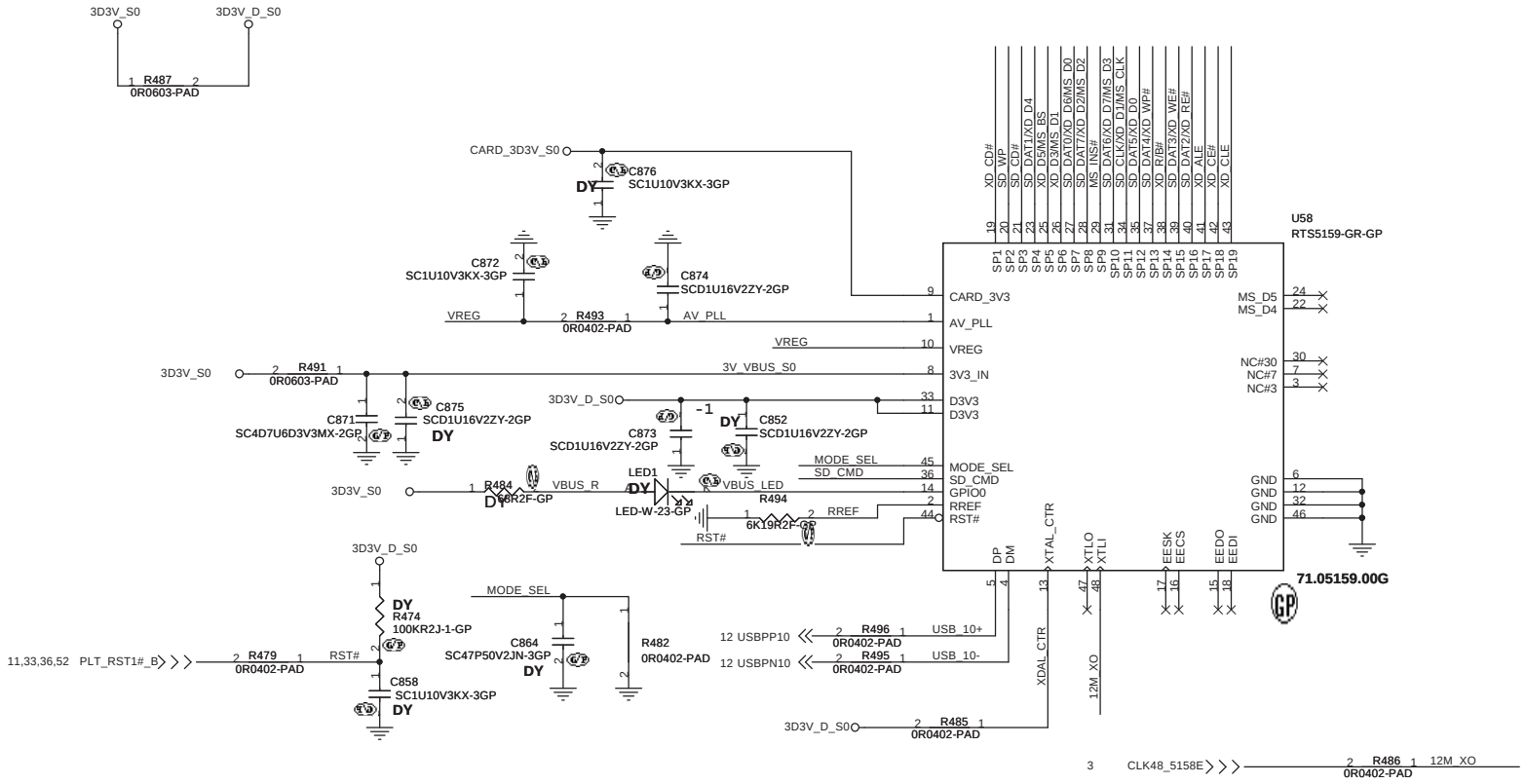
MDC 1.5 CONN



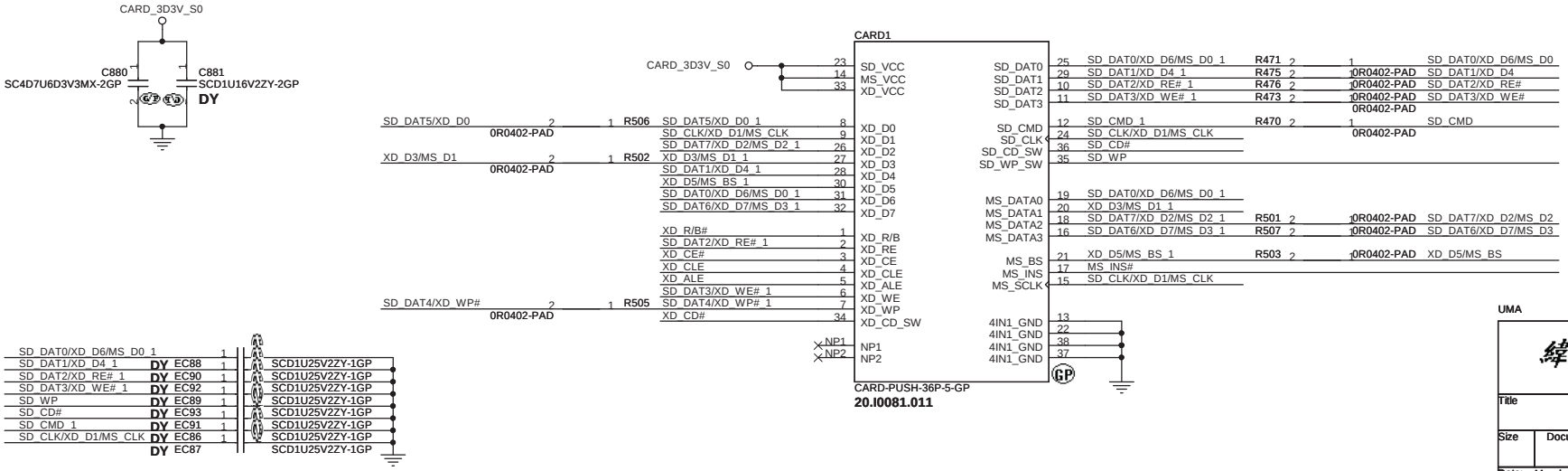


UMA

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	**MDC**	
Size	Document Number **JV71-TR**	Rev **SB**
Date: Monday, July 06, 2009	Sheet 31 of 61	



5 IN1 CARD-READER (SD/MMC/MS/MS PRO/XD)



UMA

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **CARDREADER- RTS5159**

Size	Document Number	Rev
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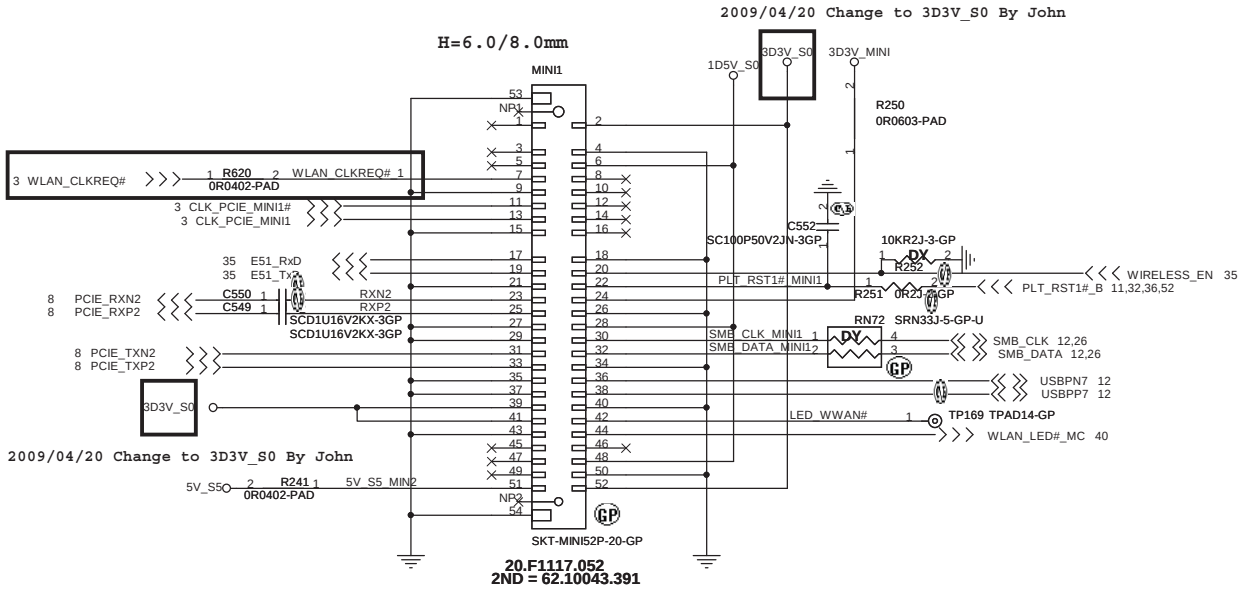
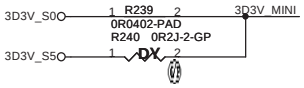
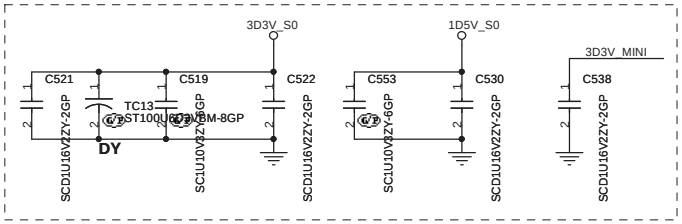
Mini Card Connector(WLAN)



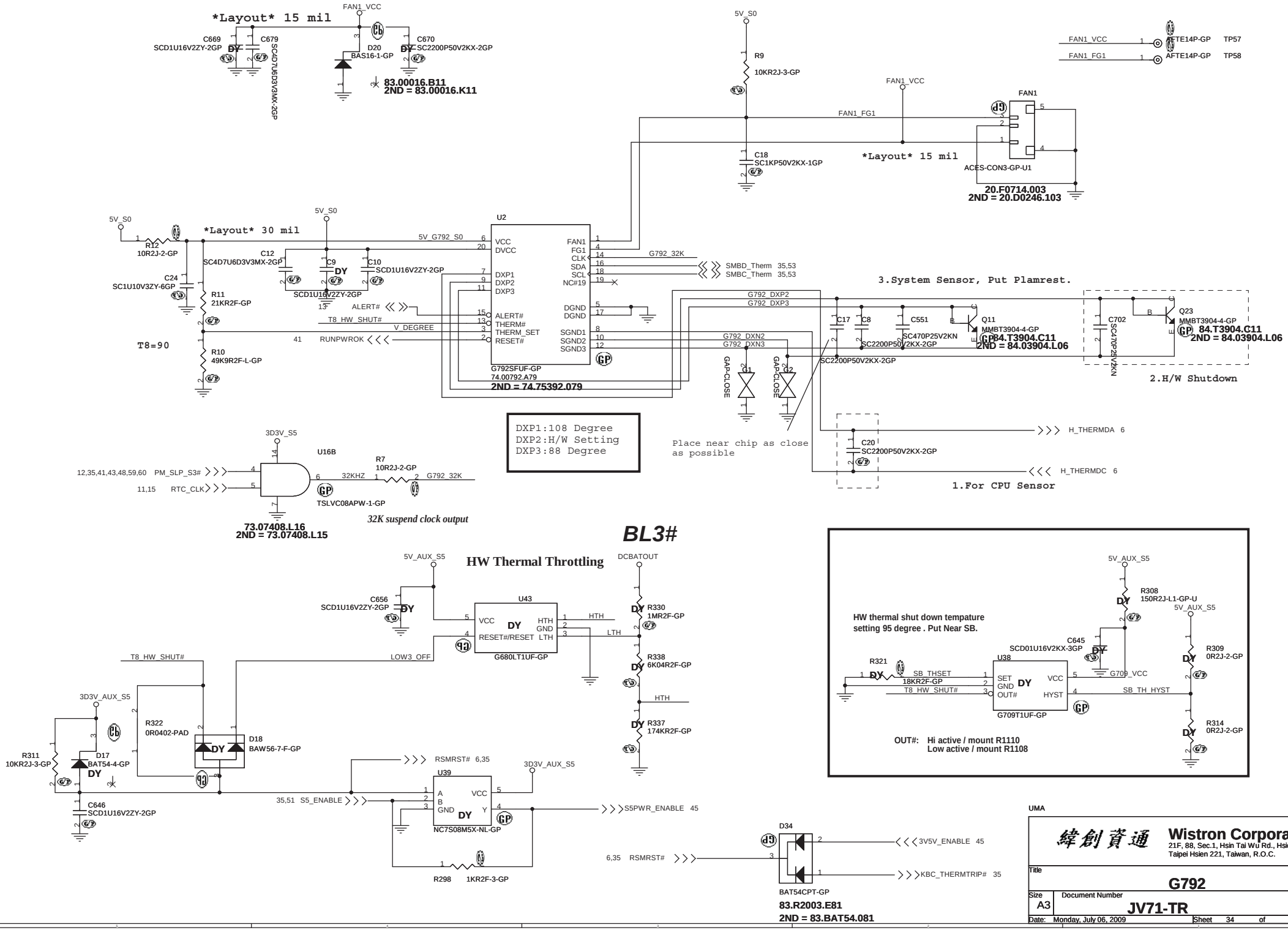


Place near MINI1



UMA

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	**MINI CARD**	
Size	Document Number **JV71-TR**	Rev **SA**
Date: Monday, July 06, 2009	Sheet 33 of 61	



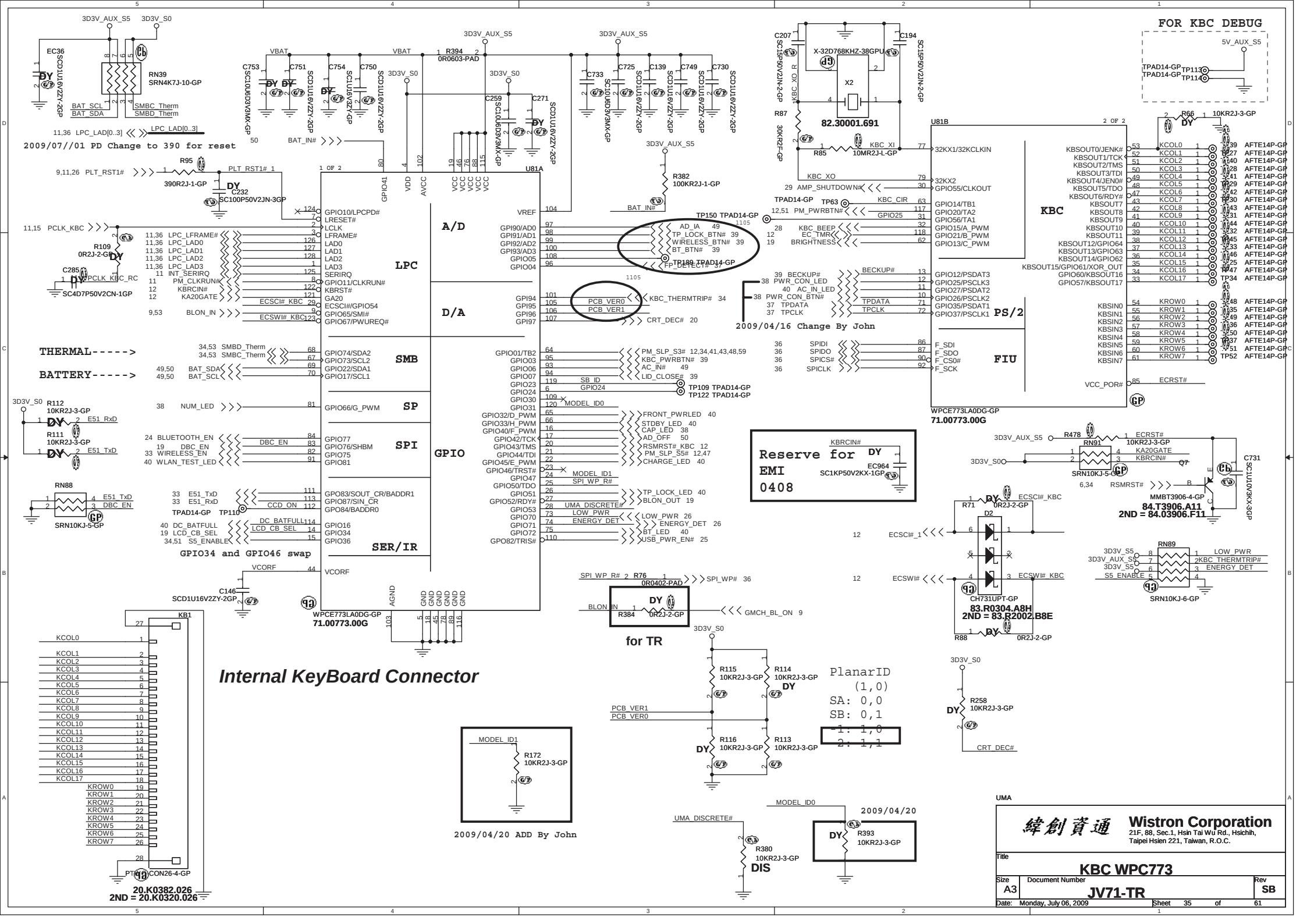
UMA

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: G792

Size: A3 | Document Number: JV71-TR | Rev: SB

Date: Monday, July 06, 2009 | Sheet 34 of 61


FOR KBC DEBUG
5V_AUX_S5
TPAD14-GP TP113
TPAD14-GP TP114
3D3V_AUX_S5 3D3V_S0
EC36 SCD1U16V2ZY-2GP
RN39 SRN4K7J-10-GP
BAT_SCL SMBC_Therm
BAT_SDA SMBD_Therm
11,36 LPC_LAD[0..3] LPC_LAD[0..3]
2009/07//01 PD Change to 390 for reset
9,11,26 PLT_RST1# R95 390R2J-1-GP PLT_RST1# 1
C232 SC100P50V2JN-3GP
11,15 PCLK_KBC
R109 0R2J-2-GP
C285 SC4D7P50V2CN-1GP
PCLK_KBC_RC
11,36 LPC_LFRAME#
11,36 LPC_LAD0
11,36 LPC_LAD1
11,36 LPC_LAD2
11,36 LPC_LAD3
11 INT_SERIRQ
11 PM_CLKRUN#
12 KBRCIN#
12 KA20GATE
ECSCI# KBC
9,53 BLON_IN
ECSWI# KBC
THERMAL----->
BATTERY----->
34,53 SMBD_Therm
34,53 SMBC_Therm
49,50 BAT_SDA
49,50 BAT_SCL
3D3V_S0 R112 10KR2J-3-GP E51_RxD
R111 10KR2J-3-GP E51_TxD
38 NUM_LED
24 BLUETOOTH_EN
19 DBC_EN
33 WIRELESS_EN
40 WLAN_TEST_LED
DBC_EN
RN88 SRN10KJ-5-GP
33 E51_TxD
33 E51_RxD
TPAD14-GP TP110
CCD_ON
40 DC_BATFULL
19 LCD_CB_SEL
34,51 S5_ENABLE
DC_BATFULL
LCD_CB_SEL
GPIO34 and GPIO46 swap
VCORF
C146 SCD1U16V2ZY-2GP
VBAT
C753 SC10U6D3V3MX-GP
C751 SCD1U16V2ZY-2GP
C754 SCD1U16V2ZY-2GP
C750 SCD1U16V2ZY-2GP
R394 0R0603-PAD
3D3V_S0
C259 SC10U6D3V3MX-GP
C271 SCD1U16V2ZY-2GP
C733 SC10U6D3V3MX-GP
C725 SCD1U16V2ZY-2GP
C139 SCD1U16V2ZY-2GP
C749 SCD1U16V2ZY-2GP
C730 SCD1U16V2ZY-2GP
50 BAT_IN#
R382 100KR2J-1-GP
BAT_IN#
U81A
1 OF 2
GPIO41 VDD AVCC VCC VCC VCC VCC VCC
80 4 102 19 46 76 88 115
LPC
A/D
D/A
SMB
SP
SPI
GPIO
SER/IR
124 GPIO10/LPCPD#
7 LRESET#
2 LCLK
3 LFRAME#
126 LAD0
127 LAD1
128 LAD2
1 LAD3
125 SERIRQ
8 GPIO11/CLKRUN#
122 KBRST#
121 GA20
29 ECSCI#/GPIO54
9 GPIO65/SMI#
123 GPIO67/PWUREQ#
68 GPIO74/SDA2
67 GPIO73/SCL2
69 GPIO22/SDA1
70 GPIO17/SCL1
81 GPIO66/G_PWM
84 GPIO77
83 GPIO76/SHBM
82 GPIO75
91 GPIO81
111 GPO83/SOUT_CR/BADDR1
113 GPIO87/SIN_CR
112 GPO84/BADDR0
114 GPIO16
14 GPIO34
15 GPIO36
44 VCORF
103 AGND
5 GND 18 GND 45 GND 78 GND 89 GND 116 GND
WPCE773LA0DG-GP
71.00773.00G
104 VREF
97 GPI90/AD0
98 GPI91/AD1
99 GPI92/AD2
100 GPI93/AD3
108 GPIO05
96 GPIO04
AD_IA 49
TP_LOCK_BTN# 39
WIRELESS_BTN# 39
BT_BTN# 39
TP150 TPAD14-GP
TP189 TPAD14-GP
FP_DETECT# 37
101 GPI94
105 GPI95
106 GPI96
107 GPI97
PCB_VER0
PCB_VER1
KBC_THERMTRIP# 34
CRT_DEC# 20
64 GPIO01/TB2
95 GPIO03
93 GPIO06
94 GPIO07
119 GPIO23
6 GPIO24
109 GPIO24
120 GPIO31
65 GPIO32/D_PWM
66 GPIO33/H_PWM
16 GPIO40/F_PWM
17 GPIO42/TCK
20 GPIO43/TMS
21 GPIO44/TDI
22 GPIO45/E_PWM
23 GPIO46/TRST#
24 GPIO47
25 GPIO50/TDO
26 GPIO51
27 GPIO52/RDY#
28 GPIO53
73 GPIO70
74 GPIO71
75 GPIO72
110 GPO82/TRIS#
SB_ID
MODEL_ID0
MODEL_ID1
SPI_WP_R#
UMA_DISCRETE#
LOW_PWR
ENERGY_DET
PM_SLP_S3# 12,34,41,43,48,59
KBC_PWRBTN# 39
AC_IN# 49
LID_CLOSE# 39
TP109 TPAD14-GP
TP122 TPAD14-GP
FRONT_PWRLED 40
STDBY_LED 40
CAP_LED 38
AD_OFF 50
RSMRST# KBC 12
PM_SLP_S5# 12,47
CHARGE_LED 40
TP_LOCK_LED 40
BLON_OUT 19
LOW_PWR 26
ENERGY_DET 26
BT_LED 40
USB_PWR_EN# 25
SPI_WP_R# 2 R76 1 0R0402-PAD
SPI_WP# 36
BLON_IN R384 0R2J-2-GP
GMCH_BL_ON 9
for TR
C207 SC15P50V2JN-2-GP
KBC_XO_R
X-32D768KHZ-38GPU
X2
C194 SC15P50V2JN-2-GP
82.30001.691
R87 30KR2F-GP
R85 10MR2J-L-GP
KBC_XI
KBC_XO
29 AMP_SHUTDOWN#
TPAD14-GP TP63
KBC_CIR
12,51 PM_PWRBTN#
GPIO25
28 KBC_BEEP
12 EC_TMR
19 BRIGHTNESS
39 BECKUP#
38 PWR_CON_LED
40 AC_IN_LED
38 PWR_CON_BTN#
37 TPDATA
37 TPCLK
BECKUP#
TPDATA
TPCLK
2009/04/16 Change By John
36 SPIDI
36 SPIDO
36 SPICS#
36 SPICLK
F_SDI
F_SDO
F_CS0#
F_SCK
U81B
2 OF 2
77 32KX1/32KCLKIN
79 32KX2
30 GPIO55/CLKOUT
63 GPIO14/TB1
117 GPIO20/TA2
31 GPIO56/TA1
32 GPIO15/A_PWM
118 GPIO21/B_PWM
62 GPIO13/C_PWM
13 GPIO12/PSDAT3
12 GPIO25/PSCLK3
11 GPIO27/PSDAT2
10 GPIO26/PSCLK2
71 GPIO35/PSDAT1
72 GPIO37/PSCLK1
86 F_SDI
87 F_SDO
90 F_CS0#
92 F_SCK
85 VCC_POR#
ECRST#
KBC
PS/2
FIU
WPCE773LA0DG-GP
71.00773.00G
R66 10KR2J-3-GP
KBSOUT0/JENK# 53 KCOL0 1 39 AFTE14P-GP
KBSOUT1/TCK 52 KCOL1 1 27 AFTE14P-GP
KBSOUT2/TMS 51 KCOL2 1 40 AFTE14P-GP
KBSOUT3/TDI 50 KCOL3 1 28 AFTE14P-GP
KBSOUT4/JENO# 49 KCOL4 1 41 AFTE14P-GP
KBSOUT5/TDO 48 KCOL5 1 29 AFTE14P-GP
KBSOUT6/RDY# 47 KCOL6 1 42 AFTE14P-GP
KBSOUT7 43 KCOL7 1 30 AFTE14P-GP
KBSOUT8 42 KCOL8 1 43 AFTE14P-GP
KBSOUT9 41 KCOL9 1 31 AFTE14P-GP
KBSOUT10 40 KCOL10 1 44 AFTE14P-GP
KBSOUT11 39 KCOL11 1 32 AFTE14P-GP
KBSOUT12/GPIO64 38 KCOL12 1 45 AFTE14P-GP
KBSOUT13/GPIO63 37 KCOL13 1 33 AFTE14P-GP
KBSOUT14/GPIO62 36 KCOL14 1 46 AFTE14P-GP
KBSOUT15/GPIO61/XOR_OUT 35 KCOL15 1 25 AFTE14P-GP
GPIO60/KBSOUT16 34 KCOL16 1 47 AFTE14P-GP
GPIO57/KBSOUT17 33 KCOL17 1 TP34 AFTE14P-GP
KBSIN0 54 KROW0 1 48 AFTE14P-GP
KBSIN1 55 KROW1 1 35 AFTE14P-GP
KBSIN2 56 KROW2 1 49 AFTE14P-GP
KBSIN3 57 KROW3 1 36 AFTE14P-GP
KBSIN4 58 KROW4 1 50 AFTE14P-GP
KBSIN5 59 KROW5 1 37 AFTE14P-GP
KBSIN6 60 KROW6 1 51 AFTE14P-GP
KBSIN7 61 KROW7 1 TP52 AFTE14P-GP
Reserve for EMI 0408
KBRCIN#
EC964 SC1KP50V2KX-1GP
3D3V_AUX_S5 R478 10KR2J-3-GP ECRST#
RN91 SRN10KJ-5-GP
KA20GATE
KBRCIN#
3D3V_S0
6,34 RSMRST#
MMBT3906-4-GP
C731 SC1U10V3KX-3GP
84.T3906.A11
2ND = 84.03906.F11
R71 0R2J-2-GP ECSCI#_KBC
D2
12 ECSCI#_1
12 ECSWI#
ECSW# KBC
CH731UPT-GP
83.R0304.A8H
2ND = 83.R2002.B8E
R88 0R2J-2-GP
RN89 SRN10KJ-6-GP
3D3V_S5
3D3V_AUX_S5
3D3V_S5
S5_ENABLE
LOW_PWR
KBC_THERMTRIP#
ENERGY_DET
KB1
KCOL0 1
KCOL1 2
KCOL2 3
KCOL3 4
KCOL4 5
KCOL5 6
KCOL6 7
KCOL7 8
KCOL8 9
KCOL9 10
KCOL10 11
KCOL11 12
KCOL12 13
KCOL13 14
KCOL14 15
KCOL15 16
KCOL16 17
KCOL17 18
KROW0 19
KROW1 20
KROW2 21
KROW3 22
KROW4 23
KROW5 24
KROW6 25
KROW7 26
27 28
PTMCON26-4-GP
20.K0382.026
2ND = 20.K0320.026
Internal KeyBoard Connector
R115 10KR2J-3-GP
R114 10KR2J-3-GP
PCB_VER1
PCB_VER0
R116 10KR2J-3-GP
R113 10KR2J-3-GP
PlanarID
(1,0)
SA: 0,0
SB: 0,1
1: 1,0
2: 1,1
3D3V_S0
R258 10KR2J-3-GP
CRT_DEC#
MODEL_ID1
R172 10KR2J-3-GP
2009/04/20 ADD By John
UMA_DISCRETE#
R380 10KR2J-3-GP
DIS
MODEL_ID0
R393 10KR2J-3-GP
2009/04/20
UMA
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
KBC WPC773
Size A3
Document Number JV71-TR
Rev SB
Date: Monday, July 06, 2009
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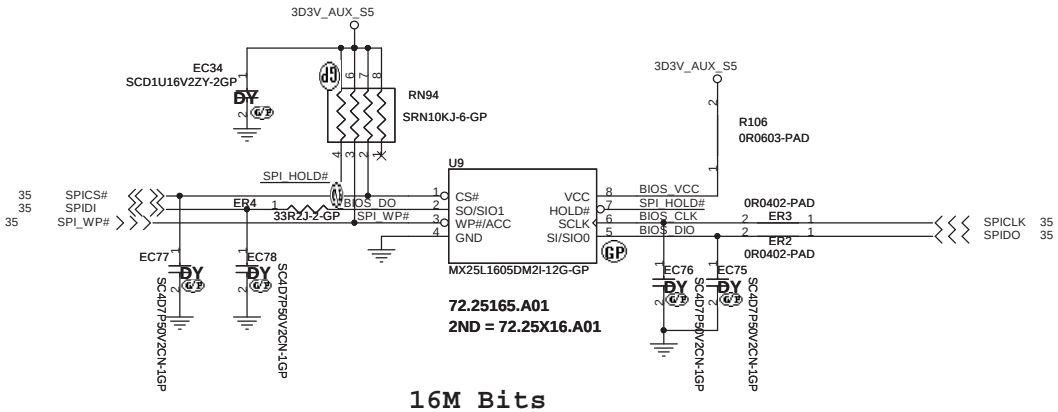
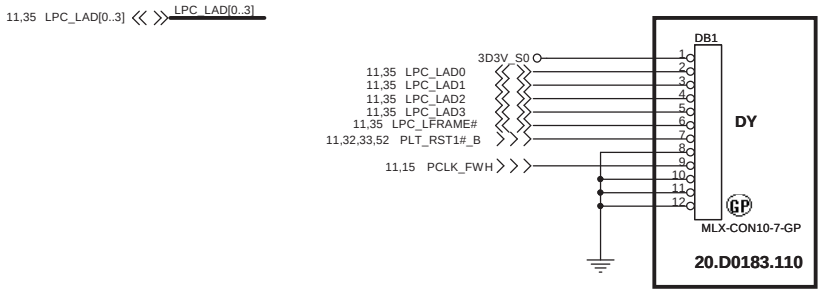


16M Bits

SPI FLASH ROM

GOLDEN FINGER FOR DEBUG BOARD



UMA

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Title		
BIOS		
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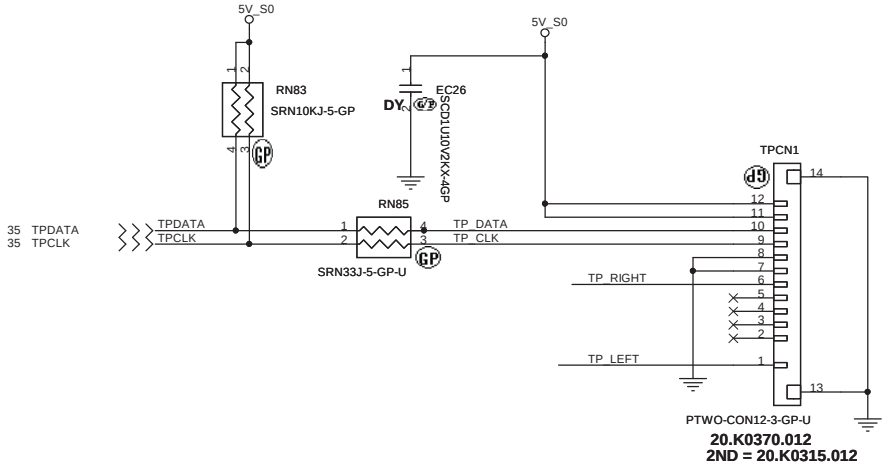
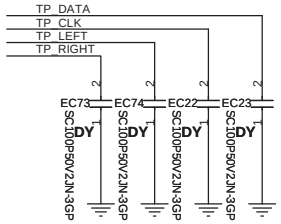
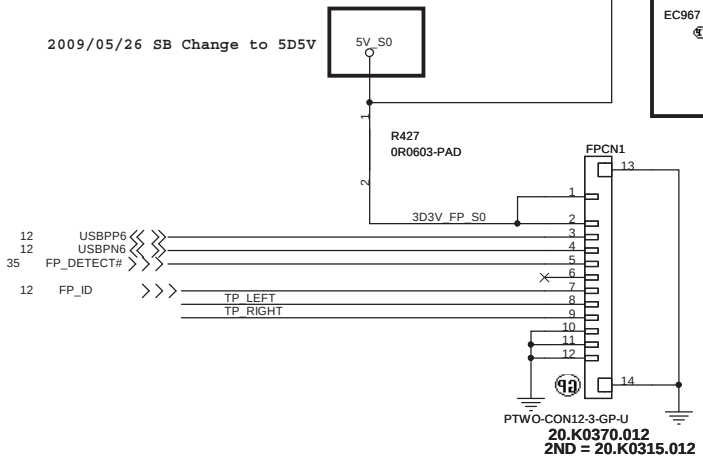
TOUCH PAD

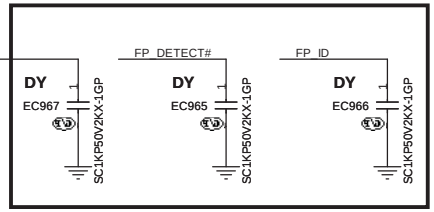




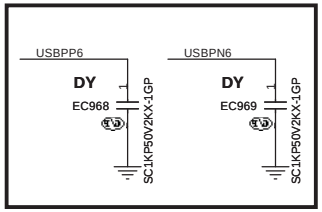
Finger printer

2009/05/26 SB Change to 5D5V





2009/04/17 For EMI By John



2009/04/21 For EMI By John

UMA

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Taipei Hsien 221, Taiwan, R.O.C.

Title		
Touch PAD/Finger printer		
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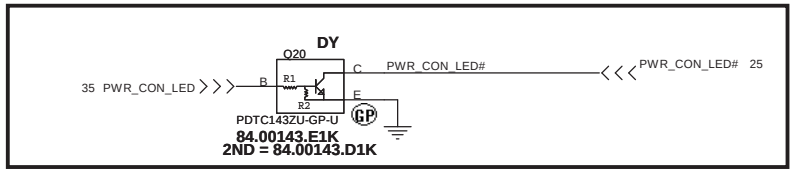
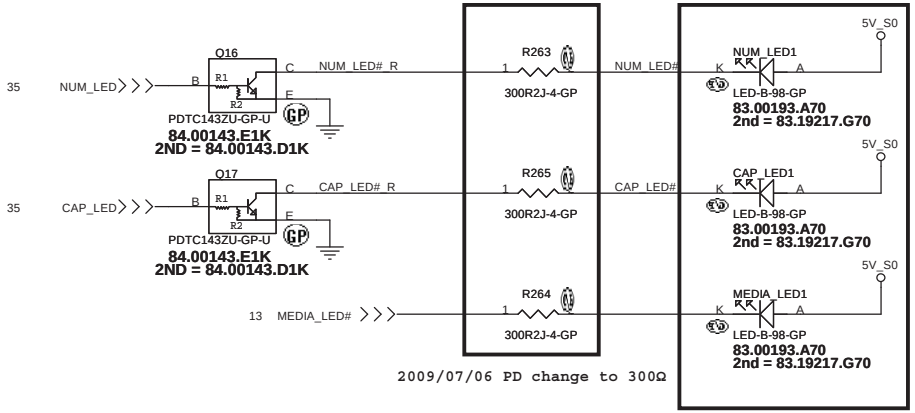
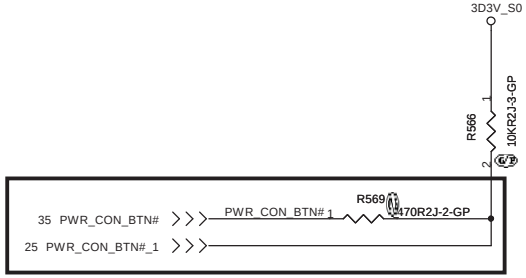
2009/04/16 Change By John

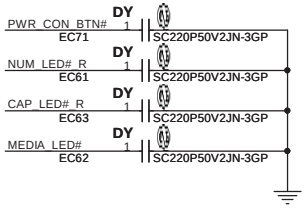




2009/07/06 PD change to 300Ω



2009/04/16 Change By John



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Taipei Hsien 221, Taiwan, R.O.C.

Title: LAUNCH BOARD

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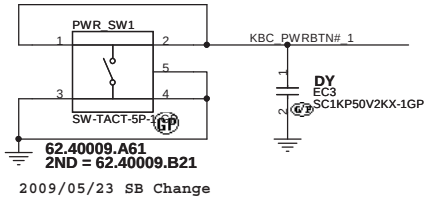
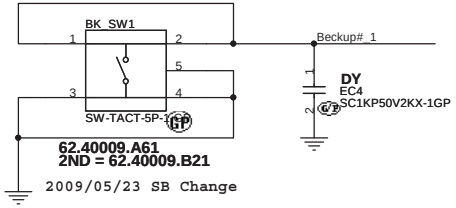
Cover Up Switch

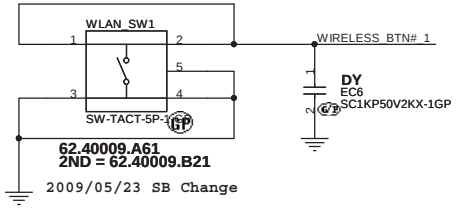
Power Button



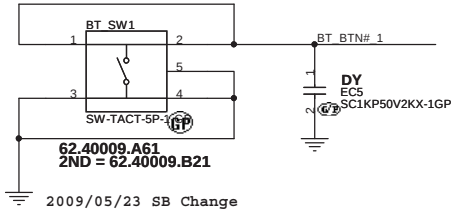
Beckup Button

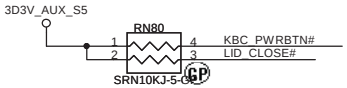


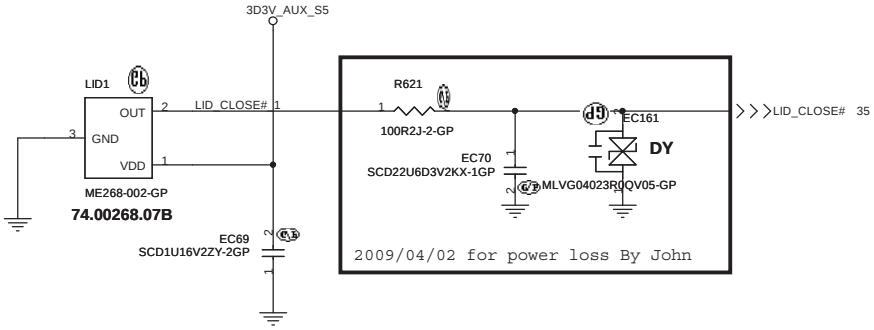
WIRELESS Button

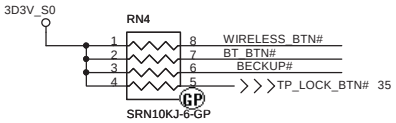


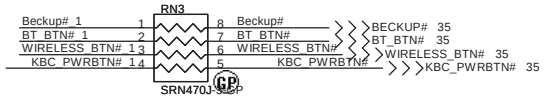
BT/3G Button



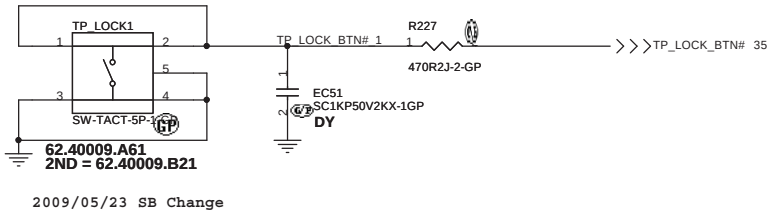








T/P lock Button



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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: SWITCH
Size: A3 | Document Number: JV71-TR | Rev: SA
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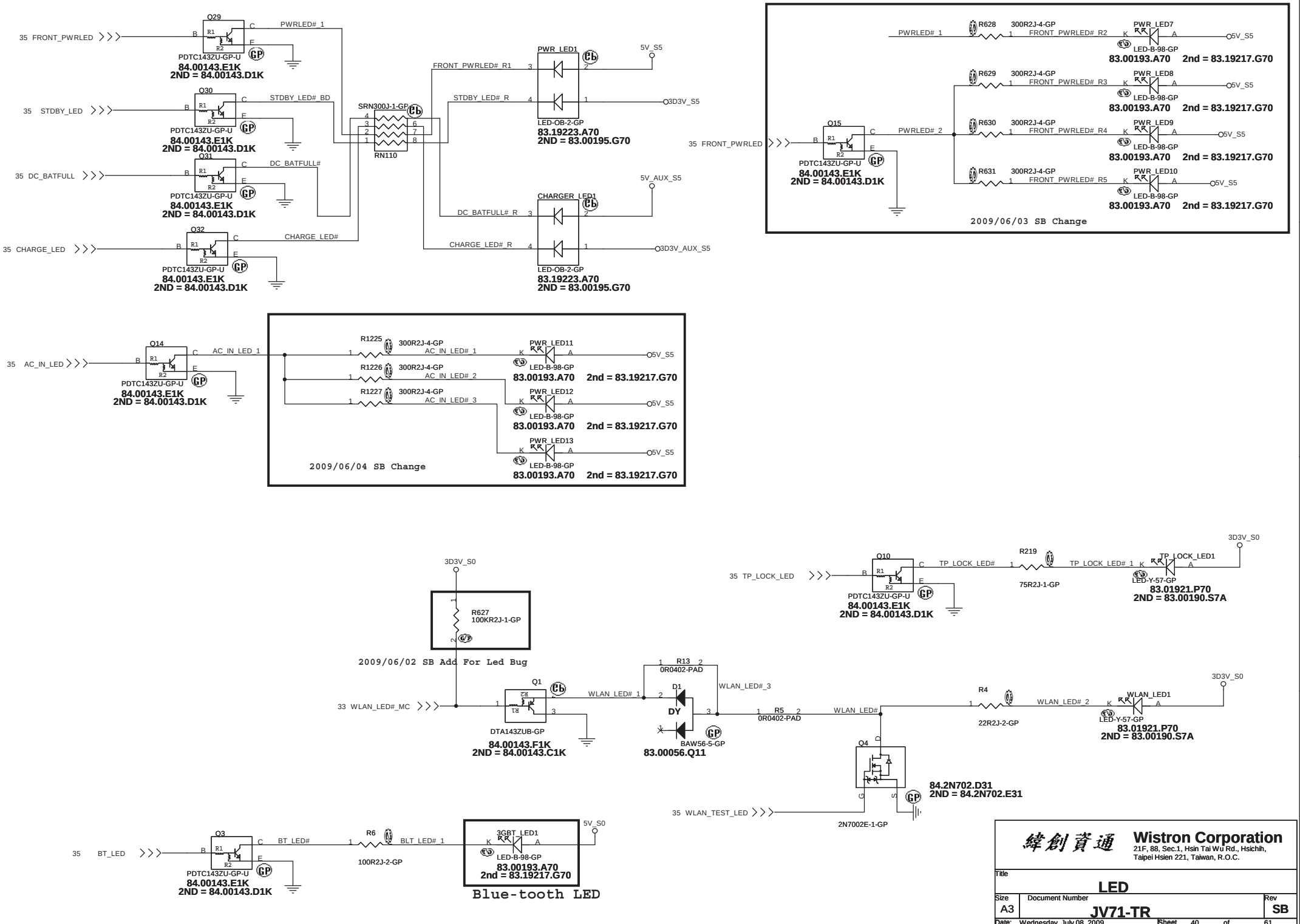
35 FRONT_PWRLED
Q29
PDTC143ZU-GP-U
84.00143.E1K
2ND = 84.00143.D1K
PWRLED# 1
35 STDBY_LED
Q30
STDBY_LED# BD
35 DC_BATFULL
Q31
DC_BATFULL#
35 CHARGE_LED
Q32
CHARGE_LED#
SRN300J-1-GP
RN110
FRONT_PWRLED# R1
STDBY_LED# R
DC_BATFULL# R
CHARGE_LED# R
PWR_LED1
LED-OB-2-GP
83.19223.A70
2ND = 83.00195.G70
5V_S5
3D3V_S5
CHARGER_LED1
5V_AUX_S5
3D3V_AUX_S5
R628
300R2J-4-GP
FRONT_PWRLED# R2
PWR_LED7
LED-B-98-GP
83.00193.A70
2nd = 83.19217.G70
R629
FRONT_PWRLED# R3
PWR_LED8
R630
FRONT_PWRLED# R4
PWR_LED9
R631
FRONT_PWRLED# R5
PWR_LED10
Q15
PWRLED# 2
2009/06/03 SB Change
35 AC_IN_LED
Q14
AC_IN_LED 1
R1225
AC_IN_LED# 1
R1226
AC_IN_LED# 2
R1227
AC_IN_LED# 3
PWR_LED11
PWR_LED12
PWR_LED13
2009/06/04 SB Change
3D3V_S0
R627
100KR2J-1-GP
2009/06/02 SB Add For Led Bug
33 WLAN_LED#_MC
Q1
DTA143ZUB-GP
84.00143.F1K
2ND = 84.00143.C1K
WLAN_LED# 1
R13
0R0402-PAD
D1
DY
BAW56-5-GP
83.00056.Q11
WLAN_LED#_3
R5
0R0402-PAD
WLAN_LED#
R4
22R2J-2-GP
WLAN_LED# 2
WLAN_LED1
LED-Y-57-GP
83.01921.P70
2ND = 83.00190.S7A
Q4
84.2N702.D31
2ND = 84.2N702.E31
35 WLAN_TEST_LED
2N7002E-1-GP
35 TP_LOCK_LED
Q10
TP_LOCK_LED#
R219
75R2J-1-GP
TP_LOCK_LED# 1
TP_LOCK_LED1
35 BT_LED
Q3
BT_LED#
R6
100R2J-2-GP
BLT_LED# 1
3GBT_LED1
5V_S0
Blue-tooth LED
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
LED
Size
A3
Document Number
JV71-TR
Rev
SB
Date: Wednesday, July 08, 2009
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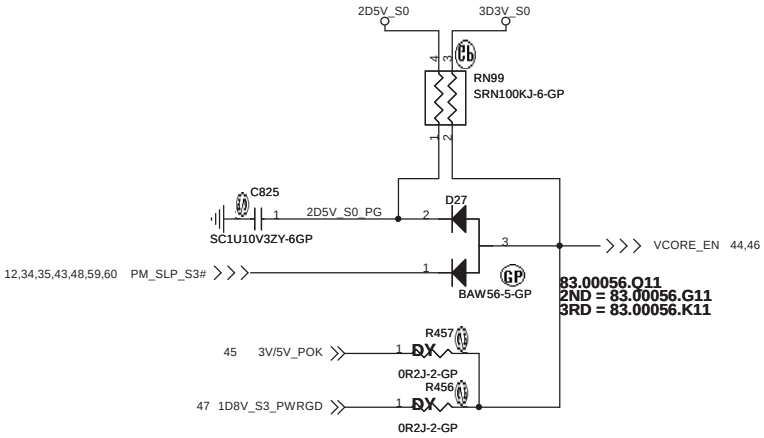
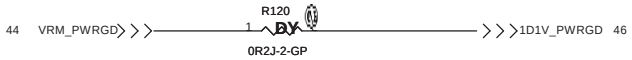
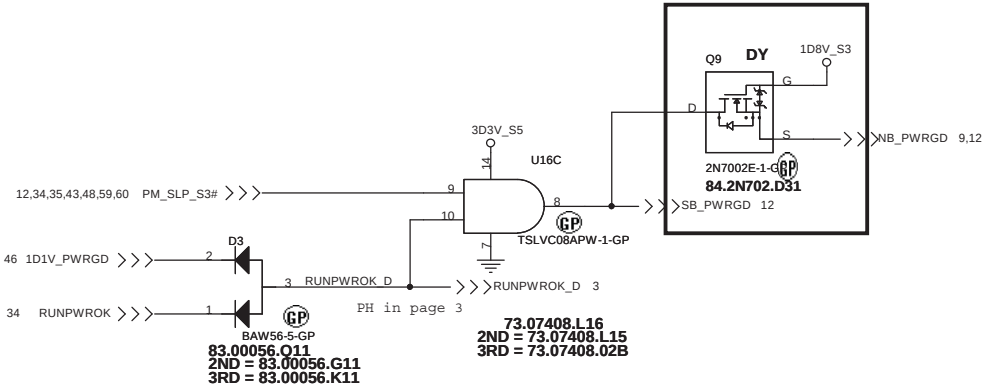


P/H @ 1D8V_S3 PAGE





UMA

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Taipei Hsien 221, Taiwan, R.O.C.

Title: **POWER ON LOGIC**

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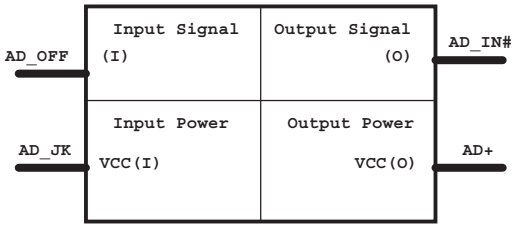
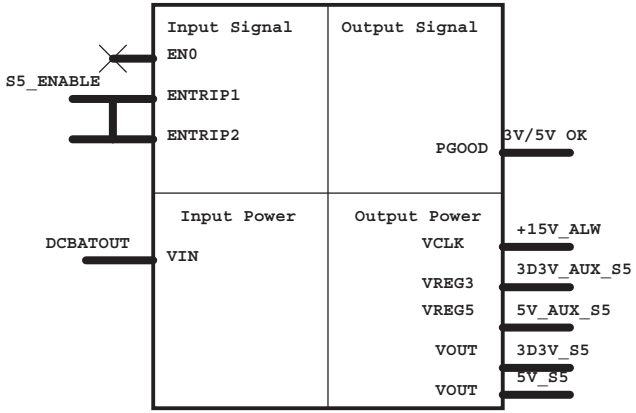
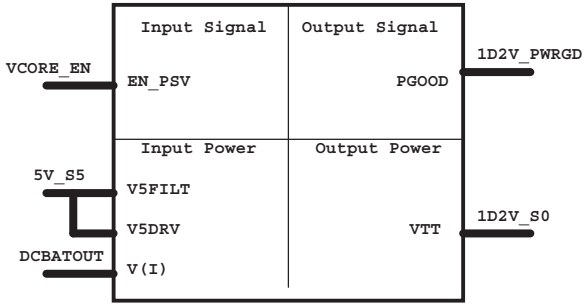
Adapter



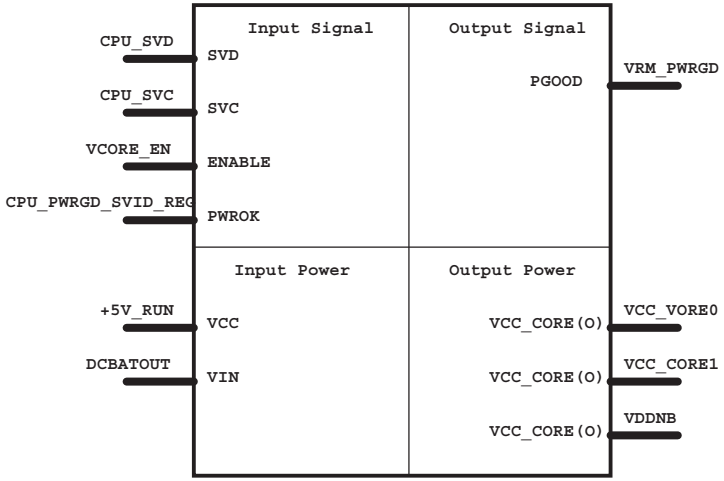
DCDC 5V/3D3V(RT8205A)



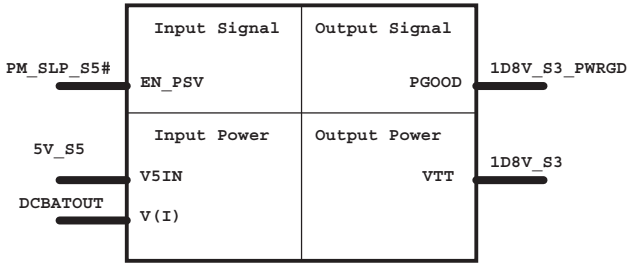
DCDC 1D2V(TPS51124)



CPU_CORE
ISL6265HRTZ



DCDC 1D8V(RT8209B)



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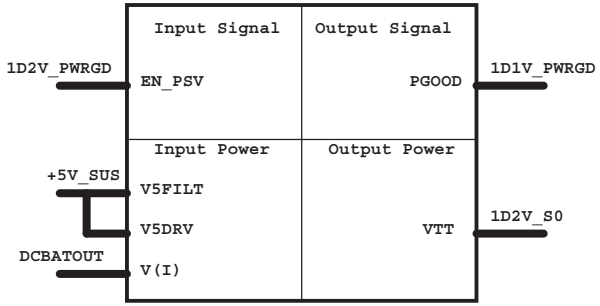
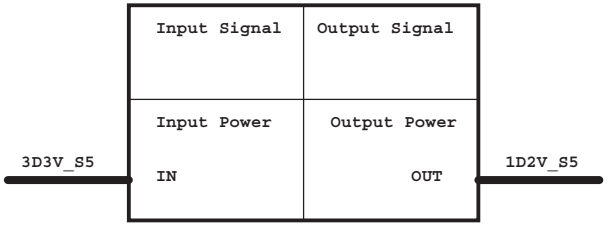
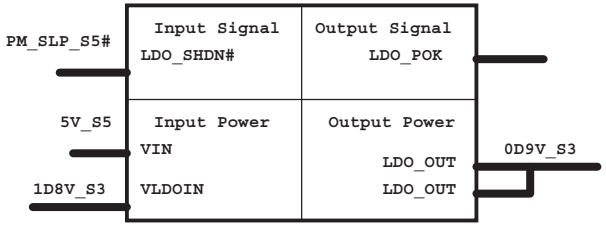


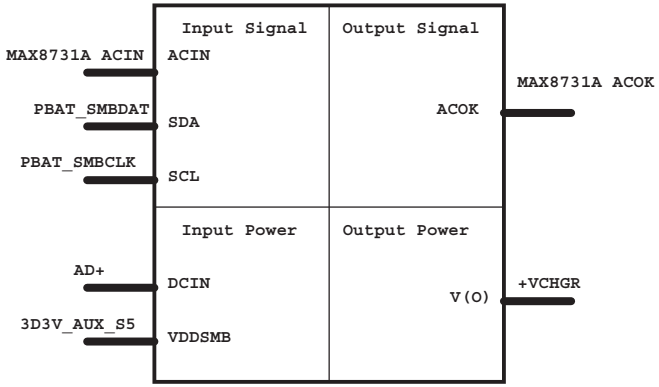
1D2V LDO G9161



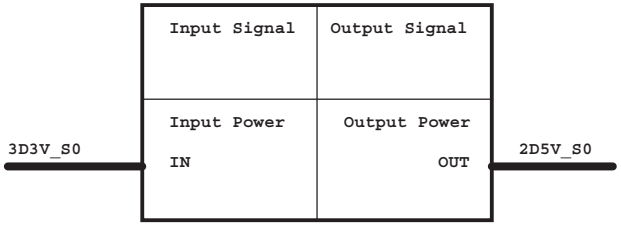
0D9V LDO RT9026



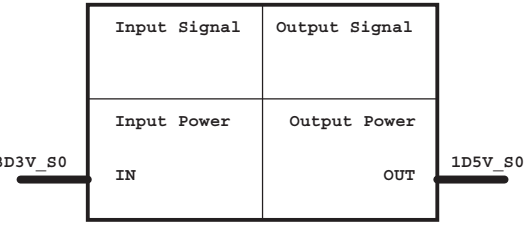
CHARGER MAX8731



2D5V LDO R9161



1D5V LDO G9571



UMA

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	Power Block Diagram	
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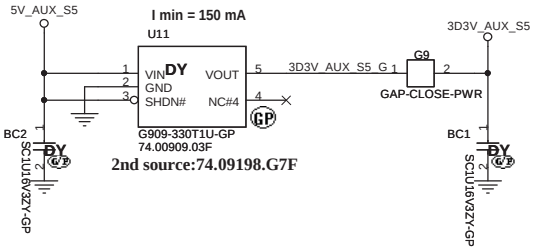
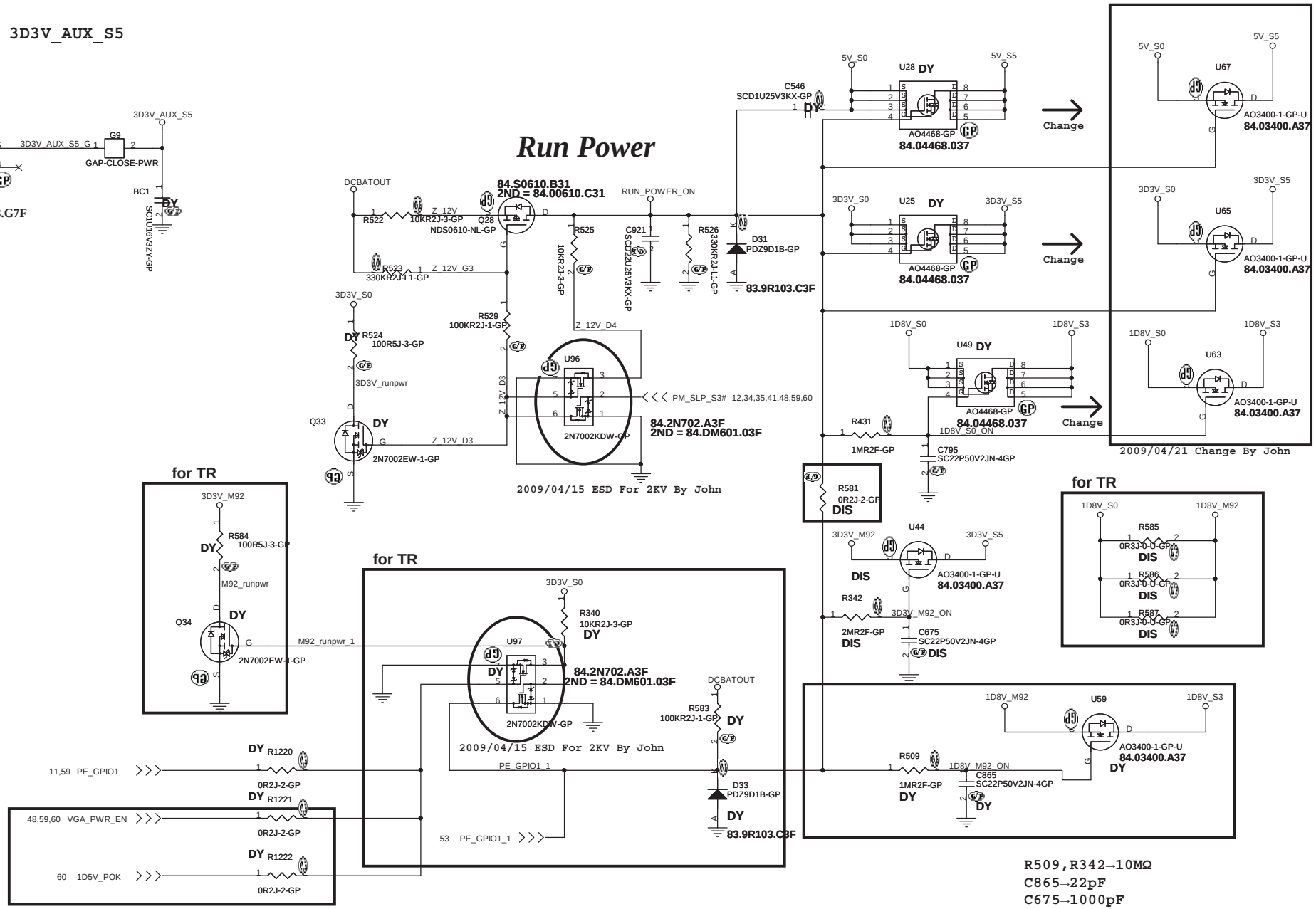
Aux Power 3D3V_AUX_S5



Run Power



R509,R342→10MΩ
C865→22pF
C675→1000pF
For VGA sequence issue

UMA

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **RUN AND AUX POWER**

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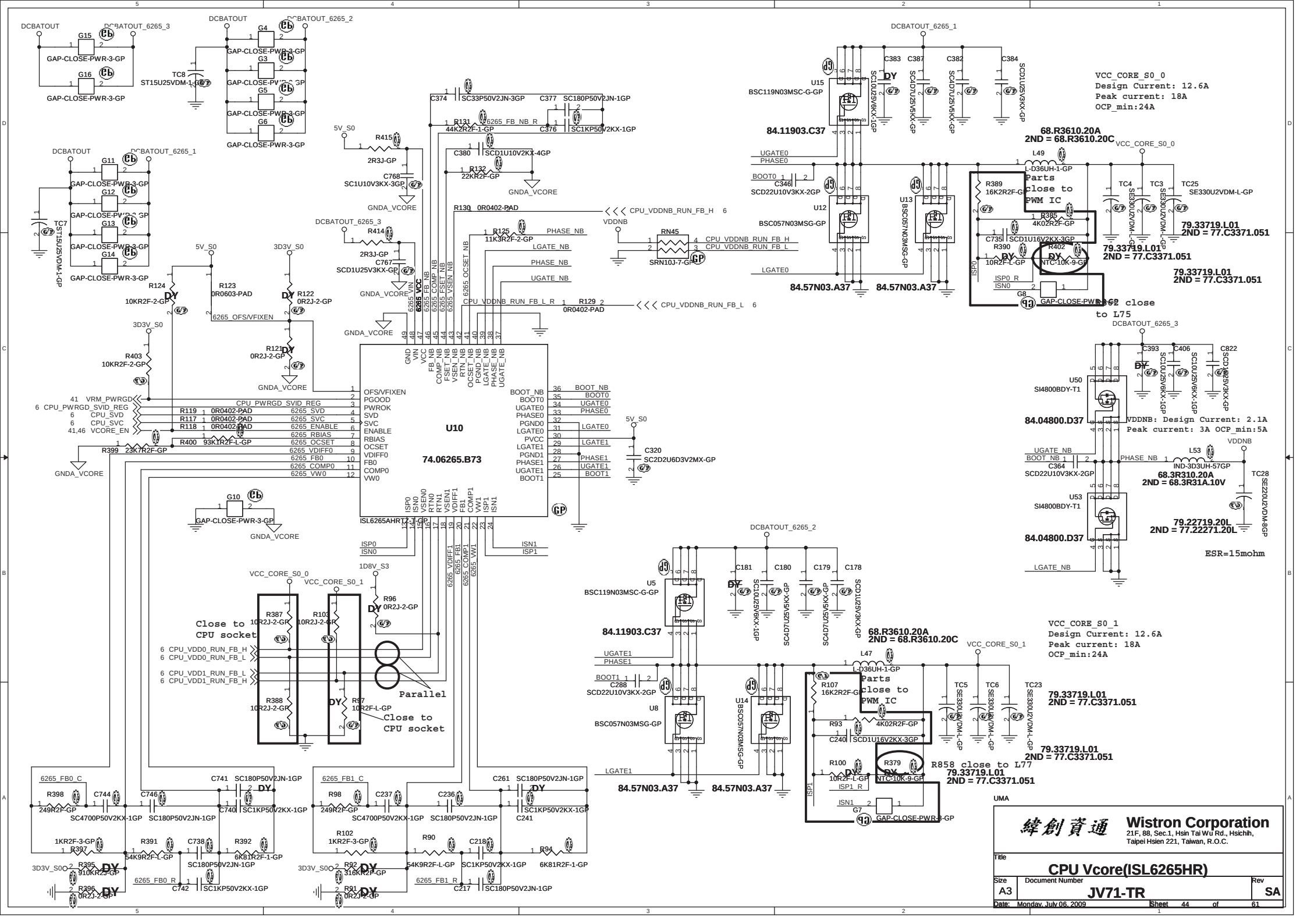
U10
74.06265.B73
ISL6265AHRTZ-T-GP
VCC_CORE_S0_0
Design Current: 12.6A
Peak current: 18A
OCP_min:24A
VCC_CORE_S0_1
Design Current: 12.6A
Peak current: 18A
OCP_min:24A
VDDNB: Design Current: 2.1A
Peak current: 3A OCP_min:5A
ESR=15mohm
Parts close to PWM IC
R858 close to L77
Close to CPU socket
Parallel
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
CPU Vcore(ISL6265HR)
JV71-TR
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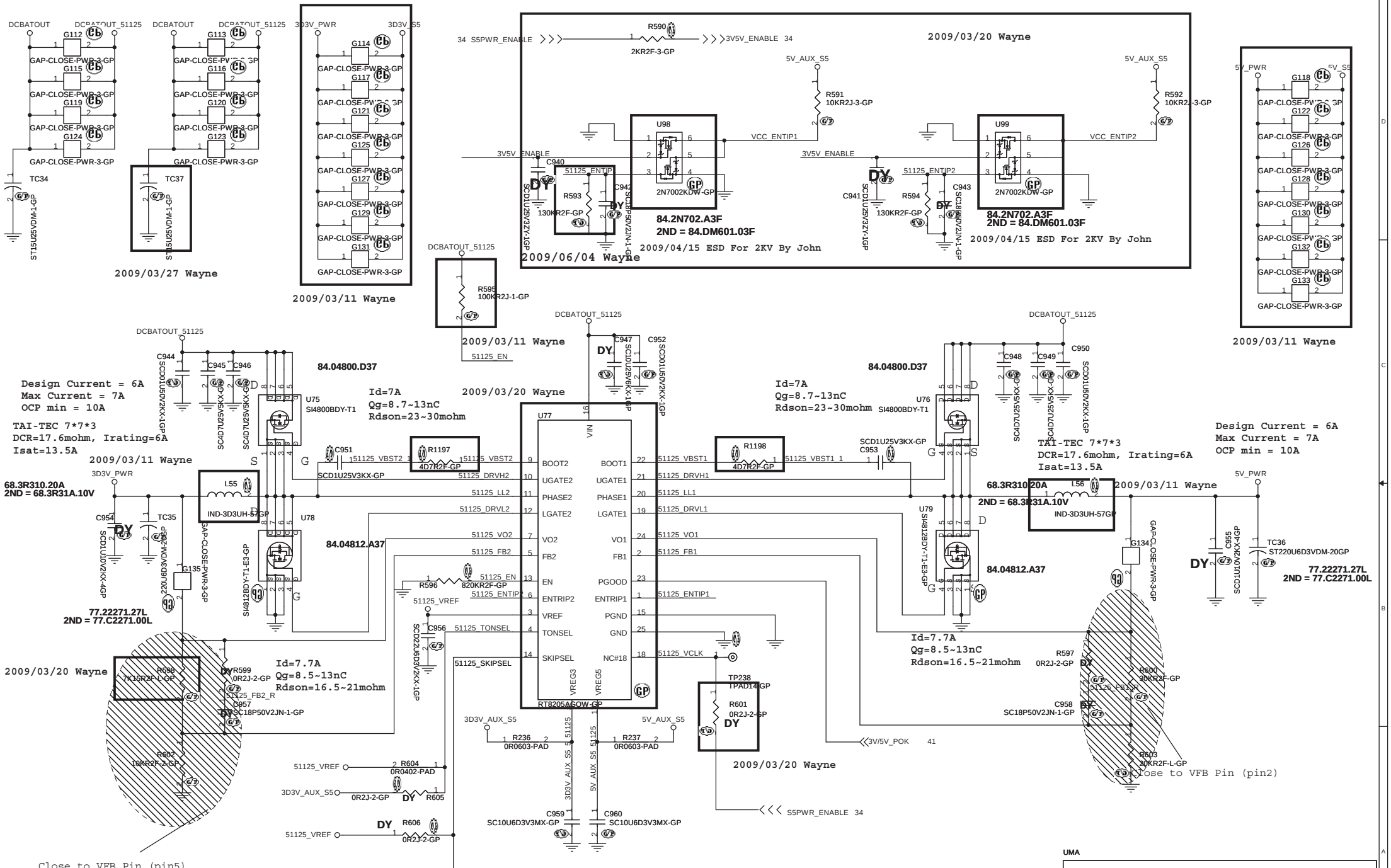
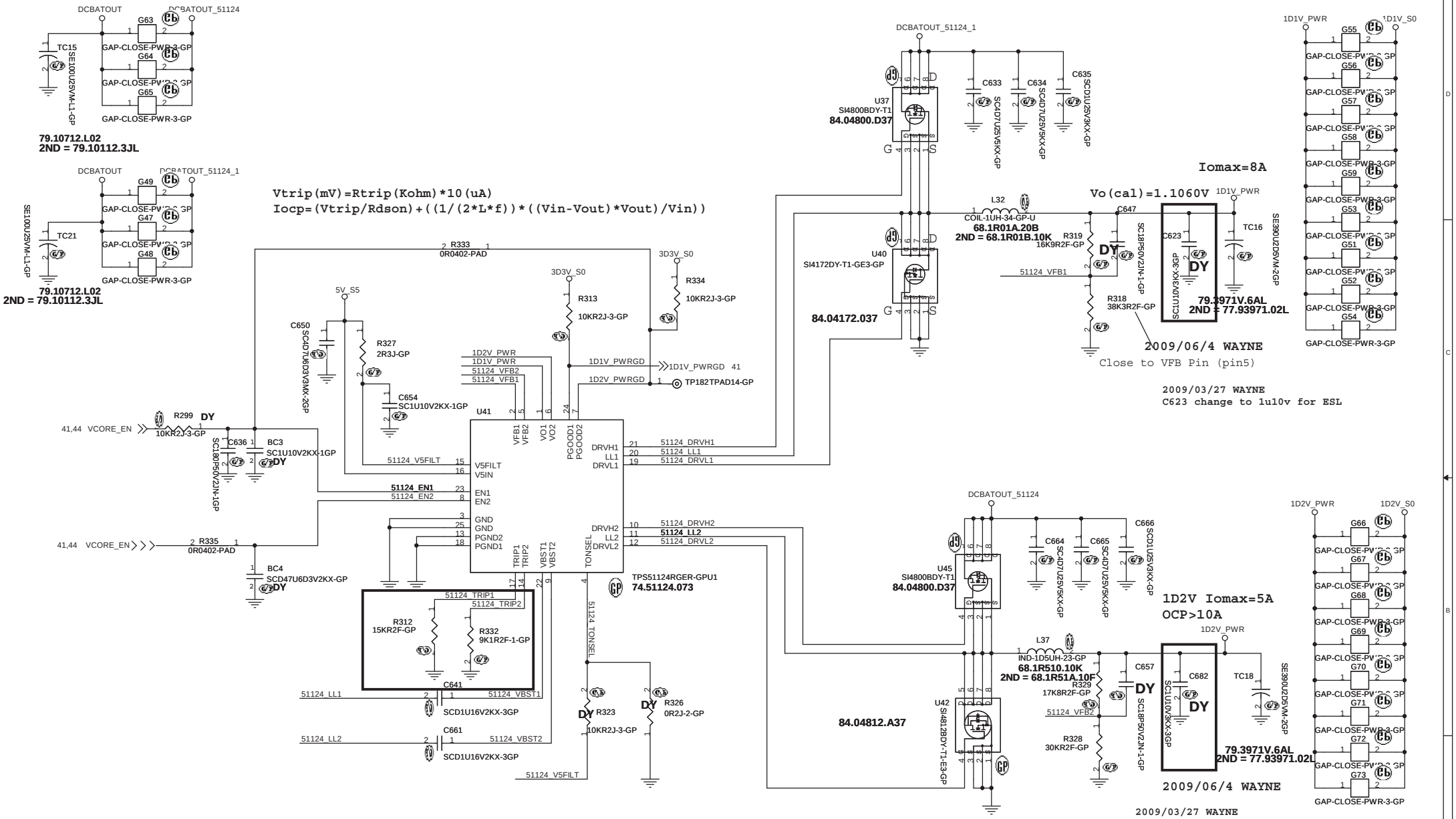

DCBATOUT
DCBATOUT_51125
3D3V_PWR
3D3V_S5
5V_PWR
5V_S5
GAP-CLOSE-PWR-3-GP
TC34
ST15U25VDM-1-GP
TC37
2009/03/27 Wayne
2009/03/11 Wayne
34 S5PWR_ENABLE
R590
2KR2F-3-GP
3V5V_ENABLE 34
2009/03/20 Wayne
5V_AUX_S5
R591
10KR2J-3-GP
R592
10KR2J-3-GP
U98
U99
VCC_ENTIP1
VCC_ENTIP2
3V5V_ENABLE
C940
51125_ENTIP
R593
130KR2F-GP
C942
SCD1U25V3KX-GP
SCD18P50V2JN-1-GP
2N7002KDW-GP
84.2N702.A3F
2ND = 84.DM601.03F
2009/04/15 ESD For 2KV By John
2009/06/04 Wayne
C941
R594
C943
DY
GP
R595
100KR2J-1-GP
51125_EN
Design Current = 6A
Max Current = 7A
OCP min = 10A
TAI-TEC 7*7*3
DCR=17.6mohm, Irating=6A
Isat=13.5A
C944
C945
C946
SCD01U50V2KX-1GP
SC4D7U25V5KX-GP
84.04800.D37
U75
SI4800BDY-T1
Id=7A
Qg=8.7~13nC
Rdson=23~30mohm
C947
C952
C948
C949
C950
U76
68.3R310.20A
2ND = 68.3R31A.10V
L55
IND-3D3UH-57GP
L56
C954
TC35
SCD01U10V2KX-4GP
220U6D3VDM-20GP
GAP-CLOSE-PWR-3-GP
G135
G134
U78
SI4812BDY-T1-E3-GP
U79
84.04812.A37
77.22271.27L
2ND = 77.C2271.00L
C951
R1197
4D7R2F-GP
R1198
SCD1U25V3KX-GP
C953
U77
VIN
BOOT2
UGATE2
PHASE2
LGATE2
VO2
FB2
EN
ENTRIP2
VREF
TONSEL
SKIPSEL
BOOT1
UGATE1
PHASE1
LGATE1
VO1
FB1
PGOOD
ENTRIP1
PGND
GND
NC#18
VREG3
VREG5
RT8205AGOW-GP
51125_VBST2
51125_DRVH2
51125_LL2
51125_DRVL2
51125_VO2
51125_FB2
51125_EN
51125_ENTIP2
51125_TONSEL
51125_SKIPSEL
51125_VBST1
51125_DRVH1
51125_LL1
51125_DRVL1
51125_VO1
51125_FB1
51125_ENTIP1
51125_VCLK
R596
820KR2F-GP
51125_VREF
C956
SCD22U6D3V2KX-1GP
R598
7K15R2F-L-GP
R599
0R2J-2-GP
51125_FB2_R
C957
SC18P50V2JN-1-GP
R602
10KR2F-2-GP
Id=7.7A
Qg=8.5~13nC
Rdson=16.5~21mohm
Close to VFB Pin (pin5)
TP238
TPAD14-GP
R601
0R2J-2-GP
3V/5V_POK 41
R597
0R2J-2-GP
R600
30KR2F-GP
C958
SC18P50V2JN-1-GP
R603
30KR2F-L-GP
Close to VFB Pin (pin2)
C955
TC36
ST220U6D3VDM-20GP
3D3V_AUX_S5
5V_AUX_S5
R236
0R0603-PAD
R237
0R0603-PAD
51125_VREF
R604
0R0402-PAD
R605
0R2J-2-GP
R606
0R2J-2-GP
R607
0R0402-PAD
R608
0R2J-2-GP
C959
SC10U6D3V3MX-GP
C960
SC10U6D3V3MX-GP
S5PWR_ENABLE 34
UMA
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
DCDC 5V/3D3V (RT8205A)
Size
A3
Document Number
JV71-TR
Rev
SA
Date: Monday, July 06, 2009
Sheet 45 of 61



	GND	OPEN	V5FILT
TONSEL	240k/CH1 300k/CH2	300k/CH1 360k/CH2	360k/CH1 420k/CH2

Vout=0.758V*(R1+R2)/R2 --> PWM mode
Vout=0.764V*(R1+R2)/R2 --> Skip Mode

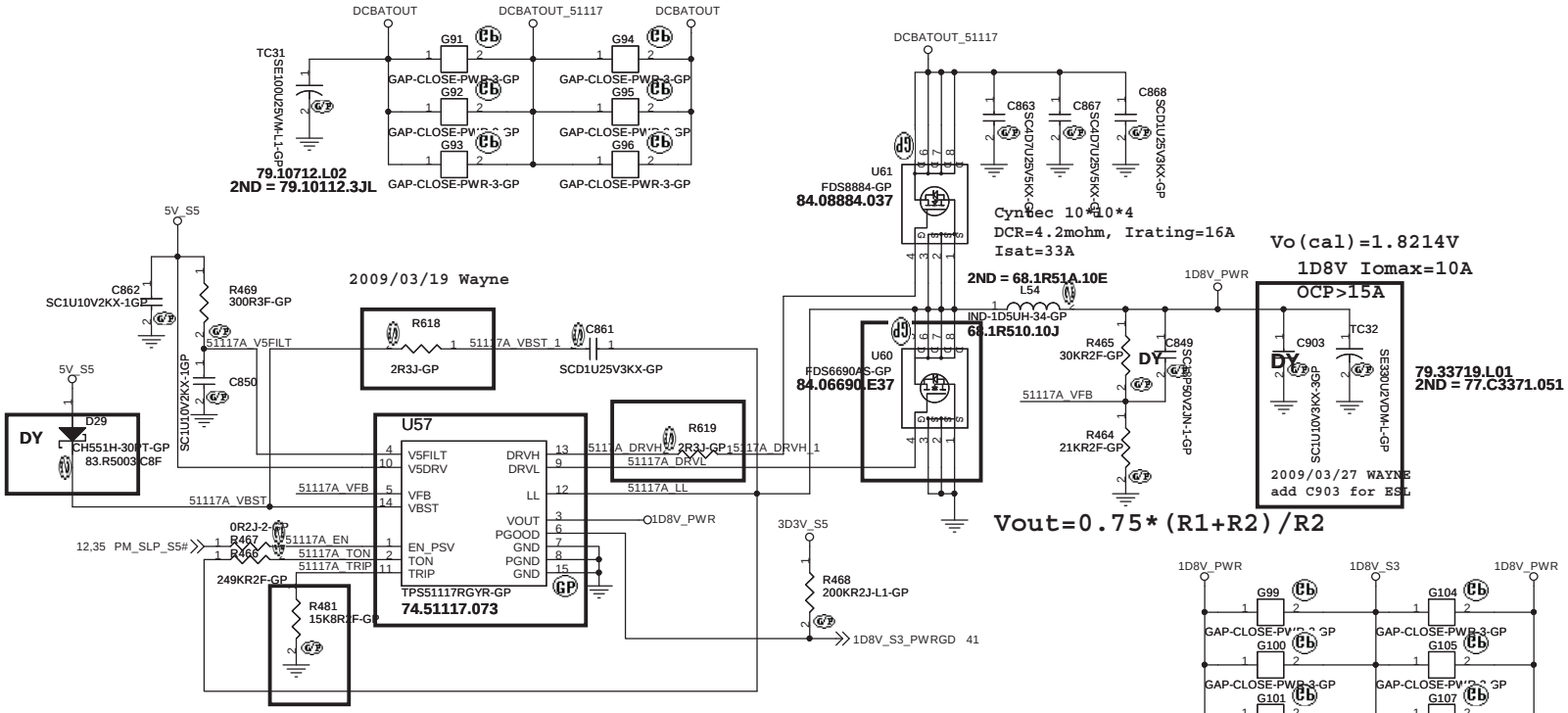
UMA

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

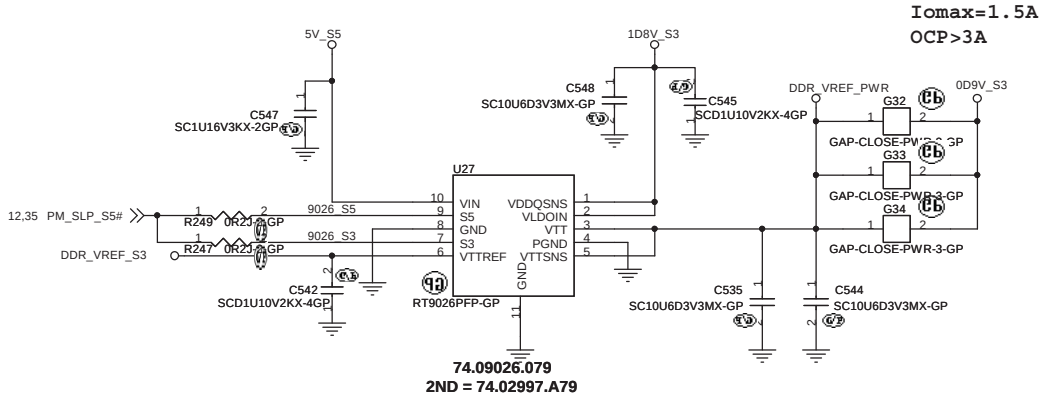
Title: *TPS51124_1D1V_1D2V*

Size	Document Number	Rev
A3	JV71-TR	SA

Date: Monday, July 06, 2009 Sheet 46 of 61

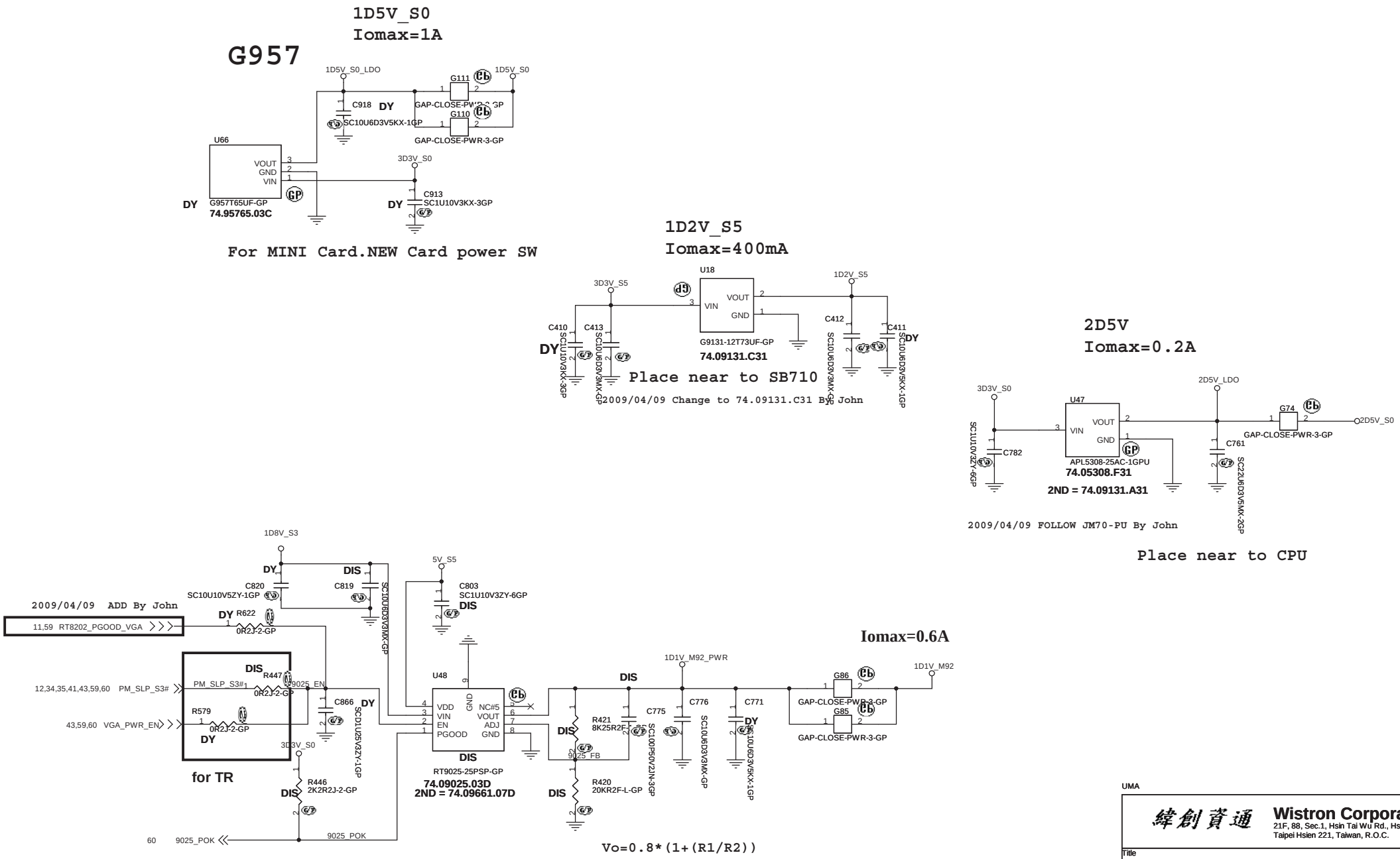


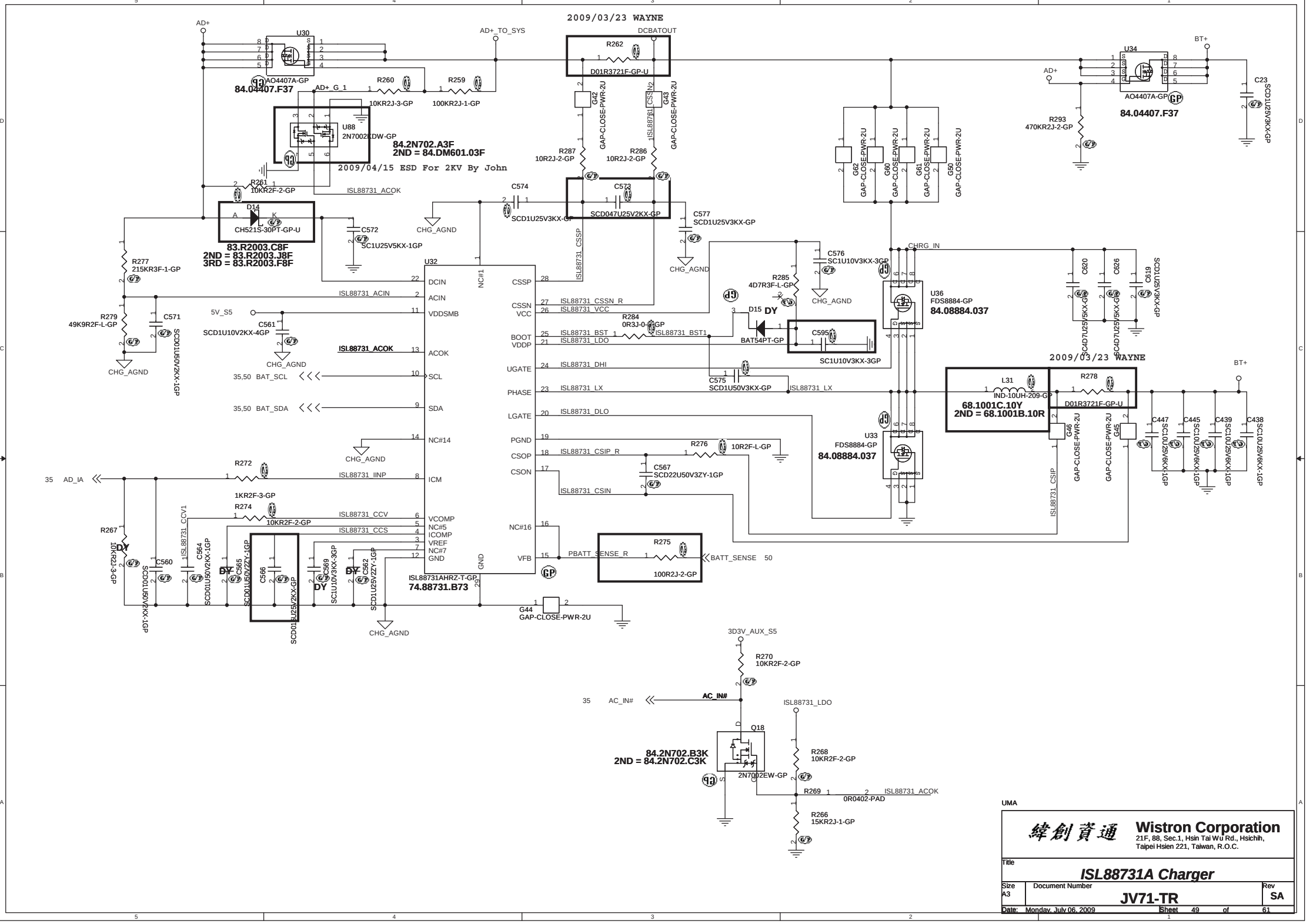
DDR_0.9V

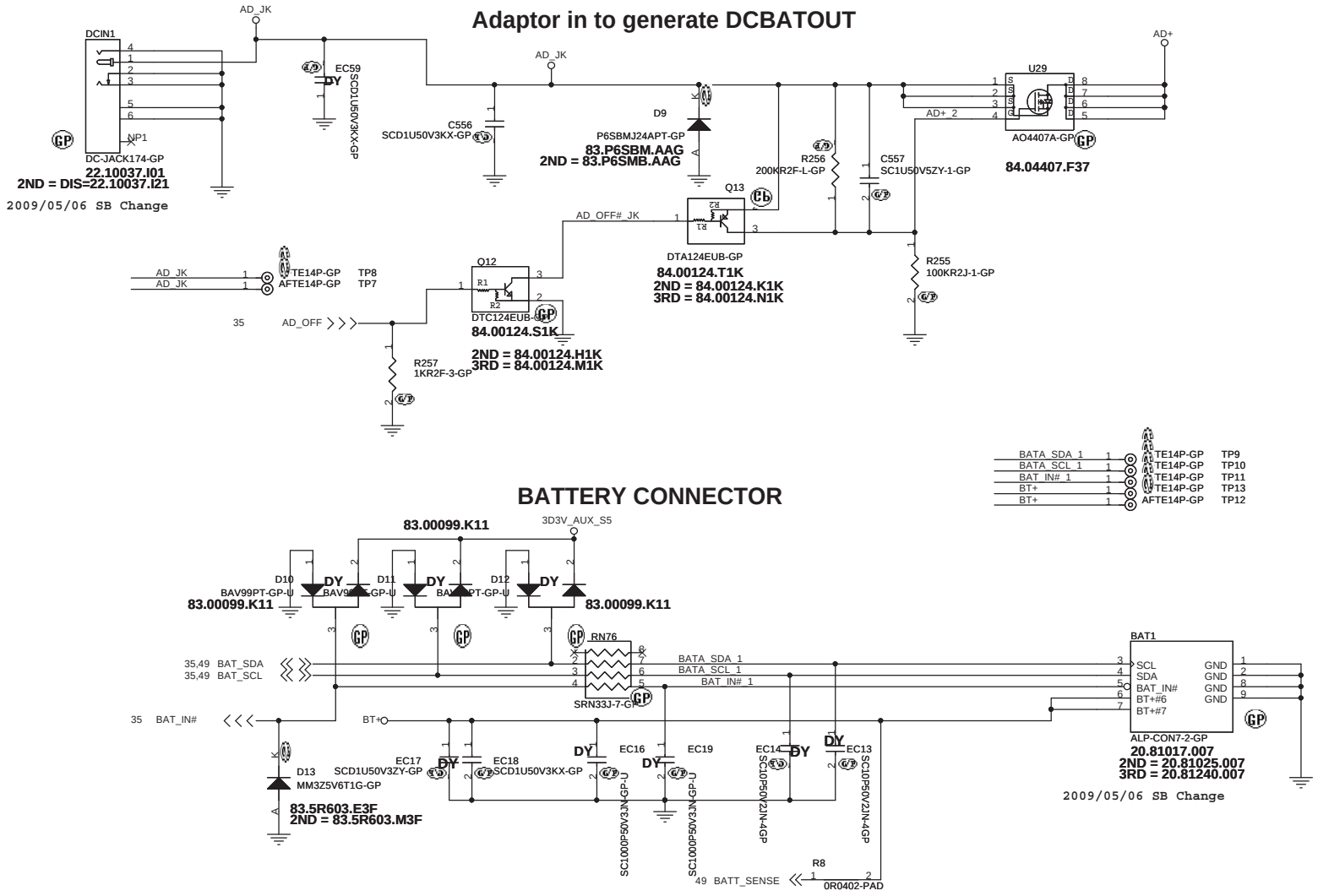


UMA

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	**DCDC_1D8V_APW7141/LDO 0D9V**
Size: A3	Document Number: **JV71-TR**	Rev: **SA**
Date: Monday, July 06, 2009	Sheet 47 of 61

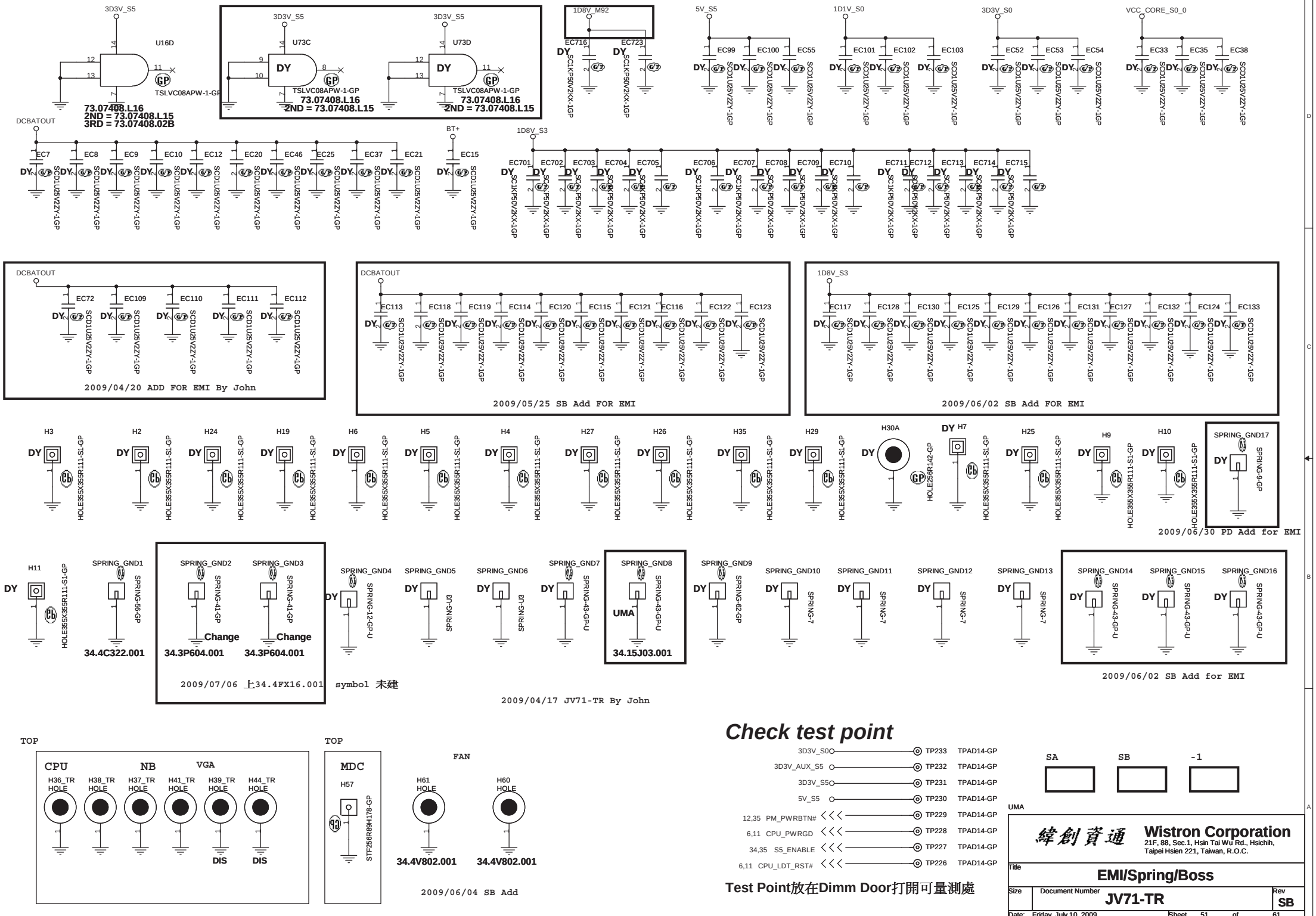

1D5V_S0
Iomax=1A
G957
1D5V_S0_LDO
1D5V_S0
G111
G110
C918
DY
SC10U6D3V5KX-1GP
GAP-CLOSE-PWR-3-GP
U66
VOUT
GND
VIN
3D3V_S0
C913
SC1U10V3KX-3GP
DY
G957T65UF-GP
74.95765.03C
For MINI Card.NEW Card power SW
1D2V_S5
Iomax=400mA
U18
3D3V_S5
1D2V_S5
C410
C413
C412
C411
DY
G9131-12T73UF-GP
74.09131.C31
Place near to SB710
2009/04/09 Change to 74.09131.C31 By John
2D5V
Iomax=0.2A
3D3V_S0
2D5V_LDO
U47
G74
2D5V_S0
C782
SC1U10V2ZY-6GP
C761
SC22U6D3V5MX-2GP
APL5308-25AC-1GPU
74.05308.F31
2ND = 74.09131.A31
2009/04/09 FOLLOW JM70-PU By John
Place near to CPU
1D8V_S3
5V_S5
C820
SC10U10V5ZY-1GP
C819
C803
SC1U10V3ZY-6GP
DIS
2009/04/09 ADD By John
11,59 RT8202_PGOOD_VGA
R622
0R2J-2-GP
12,34,35,41,43,59,60 PM_SLP_S3#
PM_SLP_S3#
R447
9025_EN
43,59,60 VGA_PWR_EN
R579
C866
SC1U25V3ZY-1GP
for TR
3D3V_S0
R446
2K2R2J-2-GP
60 9025_POK
9025_POK
U48
VDD
VIN
EN
PGOOD
GND
NC#5
VOUT
ADJ
GND
RT9025-25PSP-GP
74.09025.03D
2ND = 74.09661.07D
Iomax=0.6A
1D1V_M92_PWR
1D1V_M92
G86
G85
GAP-CLOSE-PWR-3-GP
R421
8K25R2F-L-GP
9025_FB
R420
20KR2F-L-GP
C775
SC100P50V2JN-3GP
C776
SC1U6D3V3MX-GP
C771
SC10U6D3V5KX-1GP
Vo=0.8*(1+(R1/R2))
UMA
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
LDO 2D5V/1D5V/1D2V_S5/1D1V_M92
Size
A3
Document Number
JV71-TR
Rev
SA
Date: Monday, July 06, 2009
Sheet 48 of 61

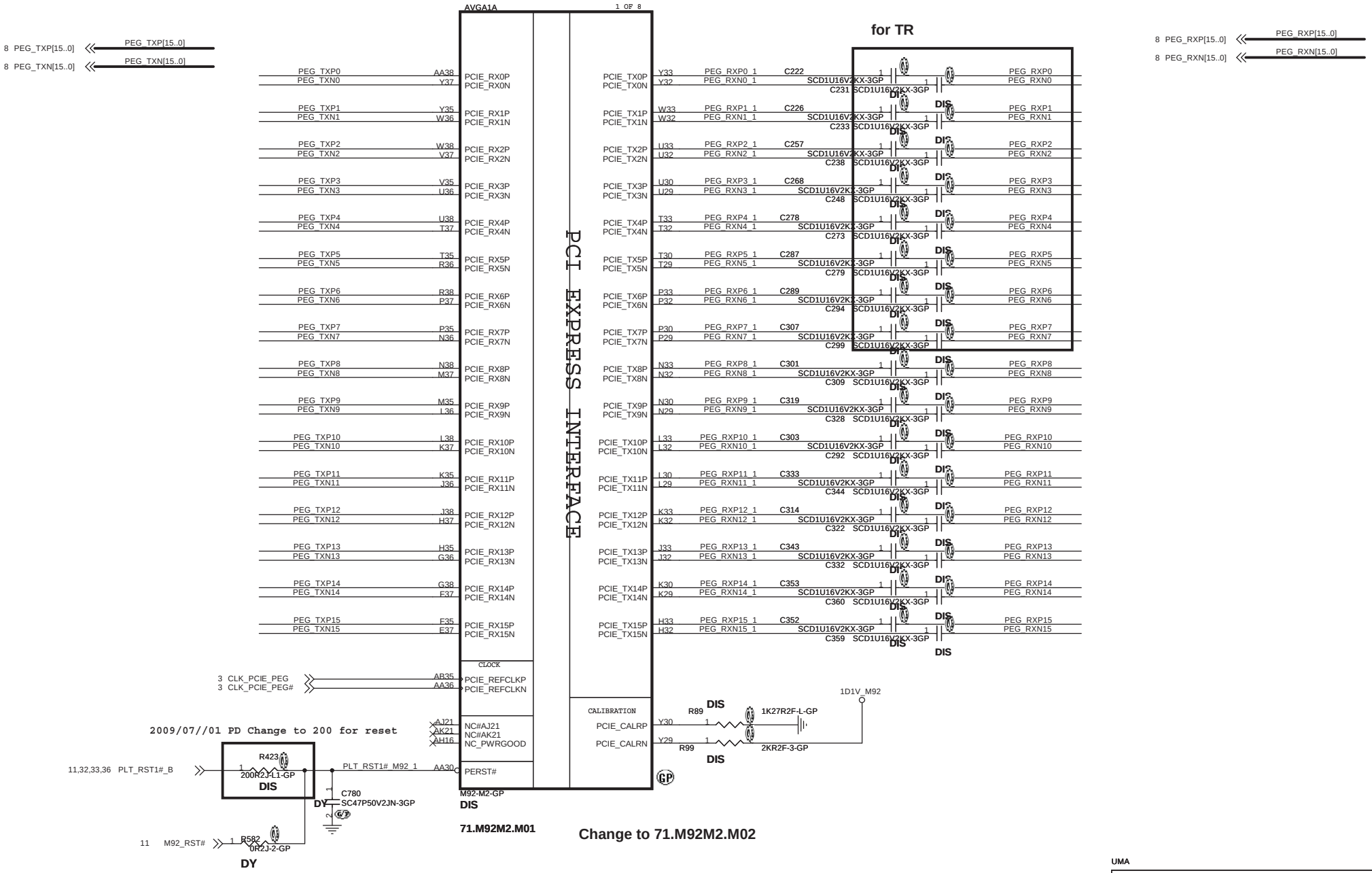

2009/03/23 WAYNE
AD+
U30
AO4407A-GP
84.04407.F37
AD+_TO_SYS
DCBATOUT
R262
D01R3721F-GP-U
R260
10KR2J-3-GP
R259
100KR2J-1-GP
AD+_G_1
U88
2N7002DW-GP
84.2N702.A3F
2ND = 84.DM601.03F
2009/04/15 ESD For 2KV By John
R261
10KR2F-2-GP
ISL88731_ACOK
D14
CH521S-30PT-GP-U
83.R2003.C8F
2ND = 83.R2003.J8F
3RD = 83.R2003.F8F
C572
SC1U25V5KX-1GP
CHG_AGND
C574
SCD1U25V3KX-GP
C573
SCD047U25V2KX-GP
C577
SCD1U25V3KX-GP
R287
10R2J-2-GP
R286
10R2J-2-GP
G42
GAP-CLOSE-PWR-2U
G43
GAP-CLOSE-PWR-2U
ISL88731_CSSN
ISL88731_CSSP
U34
AO4407A-GP
84.04407.F37
BT+
C23
SCD1U25V3KX-GP
R293
470KR2J-2-GP
G62
GAP-CLOSE-PWR-2U
G60
GAP-CLOSE-PWR-2U
G61
GAP-CLOSE-PWR-2U
G50
GAP-CLOSE-PWR-2U
R277
215KR3F-1-GP
R279
49K9R2F-L-GP
C571
SCD01U50V2KX-1GP
U32
DCIN
ACIN
VDDSMB
ACOK
SCL
SDA
NC#14
ICM
VCOMP
NC#5
ICOMP
VREF
NC#7
GND
CSSP
CSSN
VCC
BOOT
VDDP
UGATE
PHASE
LGATE
PGND
CSOP
CSON
NC#16
VFB
ISL88731AHRZ-T-GP
74.88731.B73
ISL88731_ACIN
5V_S5
C561
SCD1U10V2KX-4GP
ISL88731_ACOK
35,50 BAT_SCL
35,50 BAT_SDA
ISL88731_CSSN_R
ISL88731_VCC
ISL88731_BST
ISL88731_LDO
ISL88731_DHI
ISL88731_LX
ISL88731_DLO
ISL88731_CSIP_R
ISL88731_CSIN
R284
0R3J-0-GP
ISL88731_BST1
R285
4D7R3F-L-GP
D15
DY
BAT54PT-GP
C595
SC1U10V3KX-3GP
C576
SC1U10V3KX-3GP
C575
SCD1U50V3KX-GP
U36
FDS8884-GP
84.08884.037
U33
FDS8884-GP
84.08884.037
CHRG_IN
C620
C626
C619
SCD1U25V3KX-GP
SC4D7U25V5KX-GP
SC4D7U25V5KX-GP
2009/03/23 WAYNE
L31
IND-10UH-209-GP
68.1001C.10Y
2ND = 68.1001B.10R
R278
D01R3721F-GP-U
G46
GAP-CLOSE-PWR-2U
G45
GAP-CLOSE-PWR-2U
C447
C445
C439
C438
SCD10U25V6KX-1GP
R276
10R2F-L-GP
C567
SCD22U50V3ZY-1GP
R275
100R2J-2-GP
PBATT_SENSE_R
BATT_SENSE 50
G44
GAP-CLOSE-PWR-2U
35 AD_IA
R272
1KR2F-3-GP
R274
10KR2F-2-GP
R267
10KR2J-3-GP
C560
SCD01U50V3KX-1GP
C564
SCD01U50V2KX-1GP
C565
SCD01U50V2ZY-1GP
C566
SCD01U25V2KX-GP
C569
SC1U10V3KX-3GP
C562
SCD1U25V2ZY-1GP
3D3V_AUX_S5
R270
10KR2F-2-GP
35 AC_IN#
AC_IN#
ISL88731_LDO
Q18
84.2N702.B3K
2ND = 84.2N702.C3K
2N7002EW-GP
R268
10KR2F-2-GP
R269
0R0402-PAD
R266
15KR2J-1-GP
UMA
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
ISL88731A Charger
Size
A3
Document Number
JV71-TR
Rev
SA
Date: Monday, July 06, 2009
Sheet 49 of 61



UMA

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	**AD/BATT CONN**
Size / Document Number	**JV71-TR**
Rev	**SB**
Date: Monday, July 06, 2009	Sheet 50 of 61

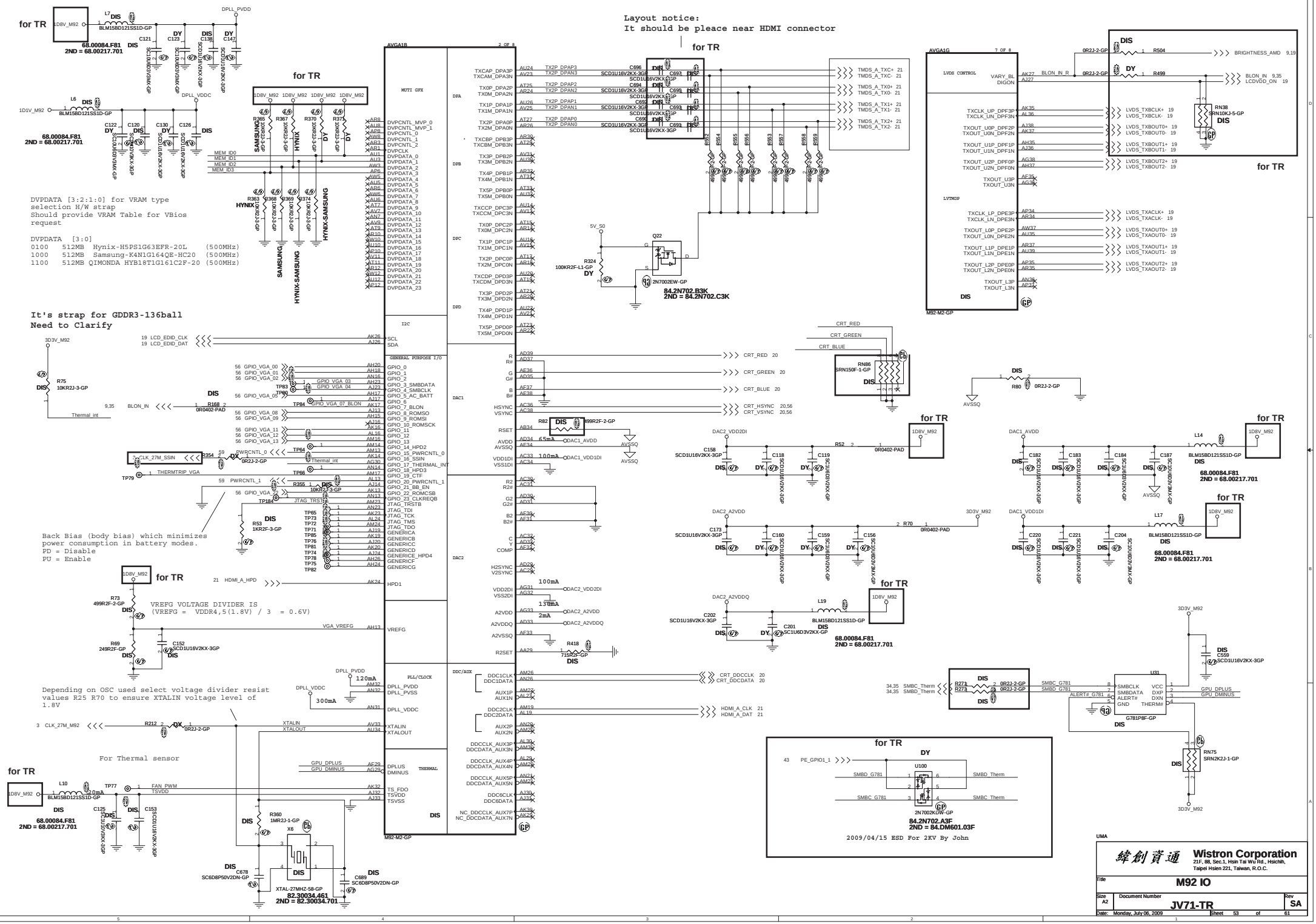

3D3V_S5
U16D
TSLVC08APW-1-GP
73.07408.L16
2ND = 73.07408.L15
3RD = 73.07408.02B
U73C
U73D
DY
1D8V_M92
EC716
EC723
SC1K250V2KX-1GP
5V_S5
EC99
EC100
EC55
SC01U25V2ZY-1GP
1D1V_S0
EC101
EC102
EC103
3D3V_S0
EC52
EC53
EC54
VCC_CORE_S0_0
EC33
EC35
EC38
DCBATOUT
EC7
EC8
EC9
EC10
EC12
EC20
EC46
EC25
EC37
EC21
BT+
EC15
1D8V_S3
EC701
EC702
EC703
EC704
EC705
EC706
EC707
EC708
EC709
EC710
EC711
EC712
EC713
EC714
EC715
EC72
EC109
EC110
EC111
EC112
2009/04/20 ADD FOR EMI By John
EC113
EC118
EC119
EC114
EC120
EC115
EC121
EC116
EC122
EC123
2009/05/25 SB Add FOR EMI
EC117
EC128
EC130
EC125
EC129
EC126
EC131
EC127
EC132
EC124
EC133
2009/06/02 SB Add FOR EMI
H3
H2
H24
H19
H6
H5
H4
H27
H26
H35
H29
H30A
H7
H25
H9
H10
HOLE355X355R111-S1-GP
HOLE256R142-GP
SPRING_GND17
SPRING-9-GP
2009/06/30 PD Add for EMI
H11
SPRING_GND1
SPRING-56-GP
34.4C322.001
SPRING_GND2
SPRING_GND3
SPRING-41-GP
Change
34.3P604.001
34.3P604.001
2009/07/06 上34.4FX16.001 symbol 未建
SPRING_GND4
SPRING-12-GP-U
SPRING_GND5
SPRING-U3
SPRING_GND6
SPRING_GND7
SPRING-43-GP-U
SPRING_GND8
UMA
34.15J03.001
SPRING_GND9
SPRING-62-GP
SPRING_GND10
SPRING_GND11
SPRING_GND12
SPRING_GND13
SPRING-7
2009/04/17 JV71-TR By John
SPRING_GND14
SPRING_GND15
SPRING_GND16
2009/06/02 SB Add for EMI
TOP
CPU
NB
VGA
H36_TR HOLE
H38_TR HOLE
H37_TR HOLE
H41_TR HOLE
H39_TR HOLE
H44_TR HOLE
DIS
MDC
H57
STF256R89H178-GP
FAN
H61 HOLE
H60 HOLE
34.4V802.001
34.4V802.001
2009/06/04 SB Add
Check test point
3D3V_S0 TP233 TPAD14-GP
3D3V_AUX_S5 TP232 TPAD14-GP
3D3V_S5 TP231 TPAD14-GP
5V_S5 TP230 TPAD14-GP
12,35 PM_PWRBTN# TP229 TPAD14-GP
6,11 CPU_PWRGD TP228 TPAD14-GP
34,35 S5_ENABLE TP227 TPAD14-GP
6,11 CPU_LDT_RST# TP226 TPAD14-GP
Test Point放在Dimm Door打開可量測處
SA
SB
-1
UMA
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
EMI/Spring/Boss
Size
Document Number
JV71-TR
Rev
SB
Date: Friday, July 10, 2009
Sheet 51 of 61

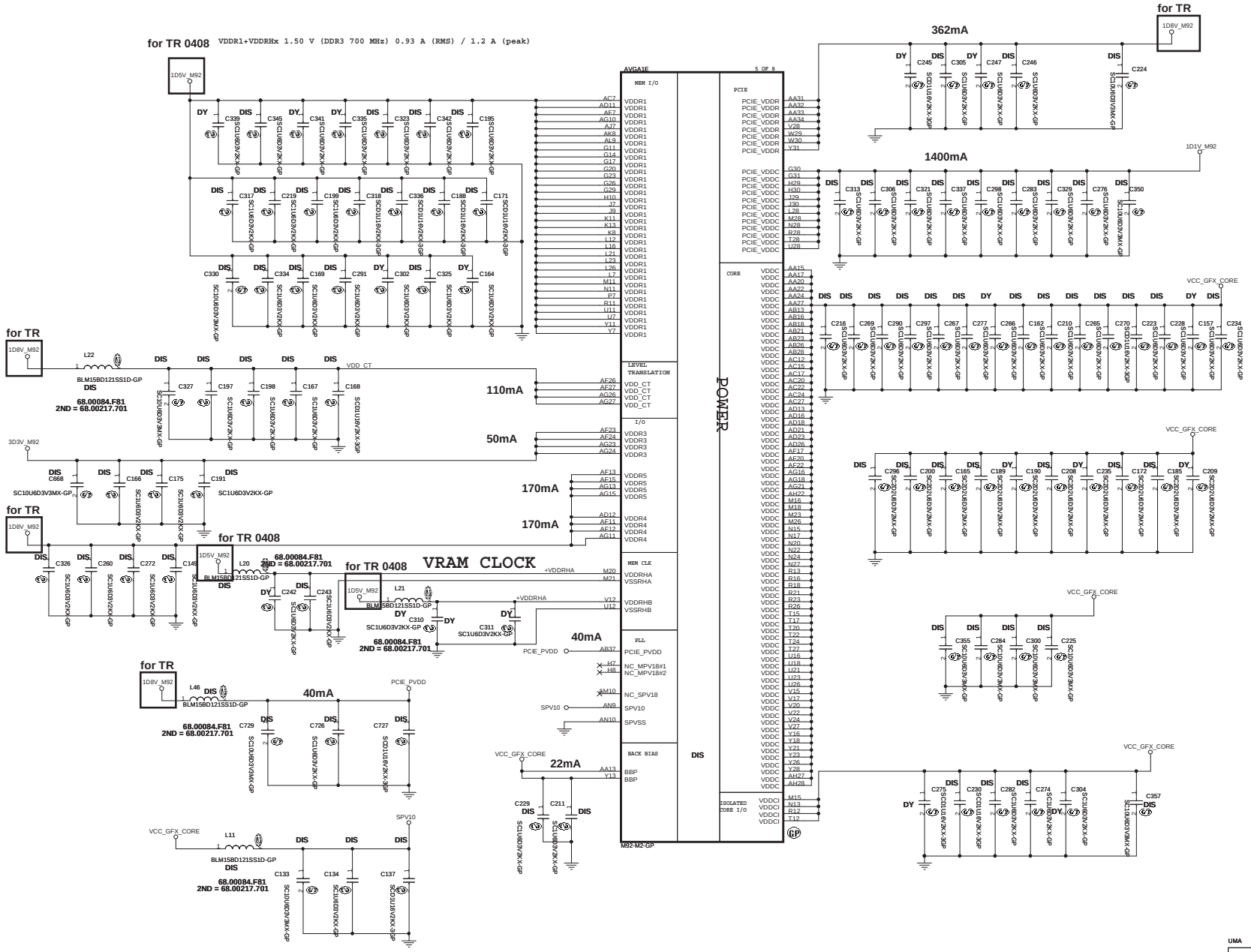


UMA

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	M92 PCIE	
Size A3	Document Number JV71-TR	Rev SB
Date: Monday, July 06, 2009	Sheet 52 of 61	


Layout notice:
It should be pleace near HDMI connector
for TR
DVPDATA [3:2:1:0] for VRAM type selection H/W strap
Should provide VRAM Table for VBios request
DVPDATA [3:0]
0100 512MB Hynix-H5PS1G63EFR-20L (500MHz)
1000 512MB Samsung-K4N1G164QE-HC20 (500MHz)
1100 512MB QIMONDA HYB18T1G161C2F-20 (500MHz)
It's strap for GDDR3-136ball
Need to Clarify
Back Bias (body bias) which minimizes power consumption in battery modes.
PD = Disable
PU = Enable
VREFG VOLTAGE DIVIDER IS
(VREFG = VDDR4,5(1.8V) / 3 = 0.6V)
Depending on OSC used select voltage divider resist values R25 R70 to ensure XTALIN voltage level of 1.8V
For Thermal sensor
2009/04/15 ESD For 2KV By John
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
M92 IO
JV71-TR
SA
Date: Monday, July 06, 2009
Sheet 53 of 61



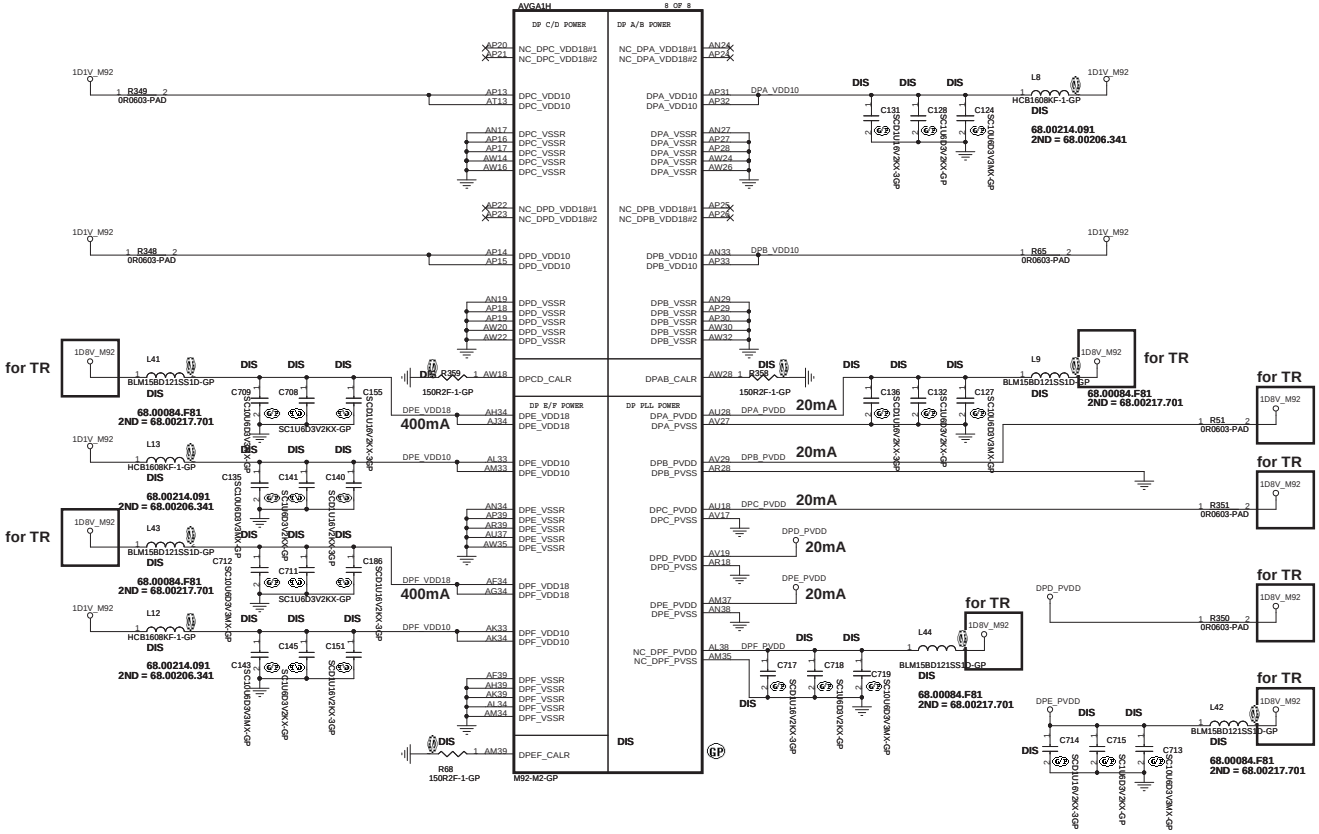
UMA

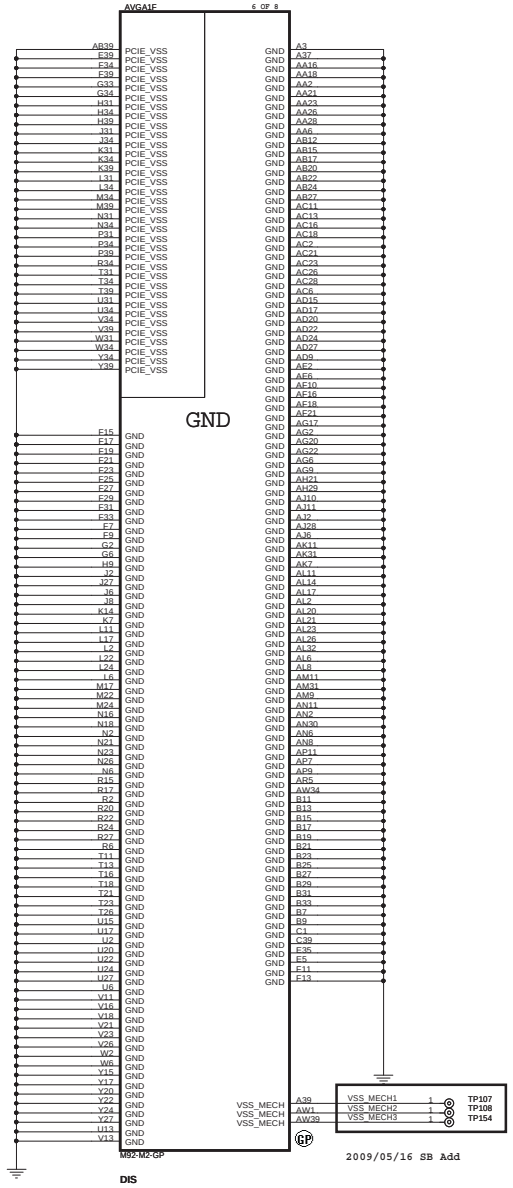
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **M92 POWER**

Size	Document Number	Rev
A2	JV71-TR	SA

Date: Monday, July 06, 2009 Sheet 54 of 61





UMA

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **DP POWER_GND**

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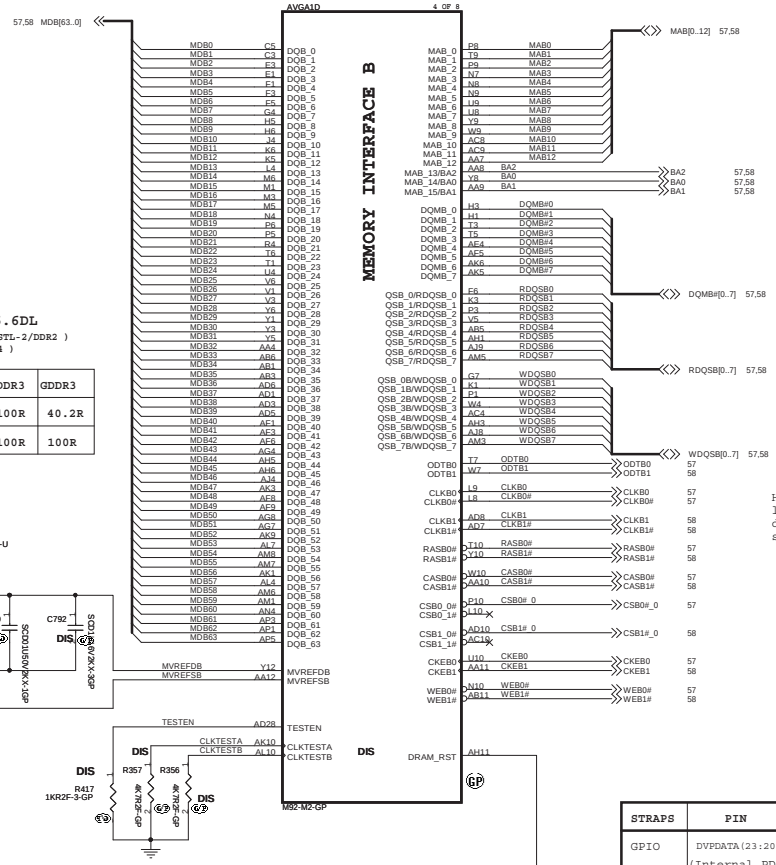
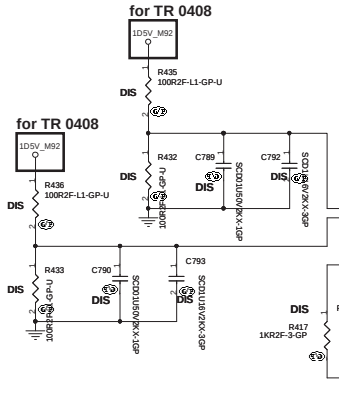
M92-M2 uses memory group B only

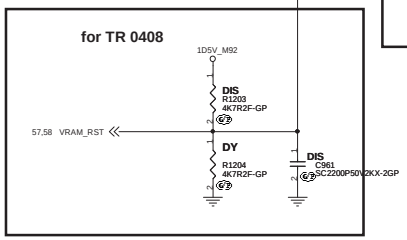


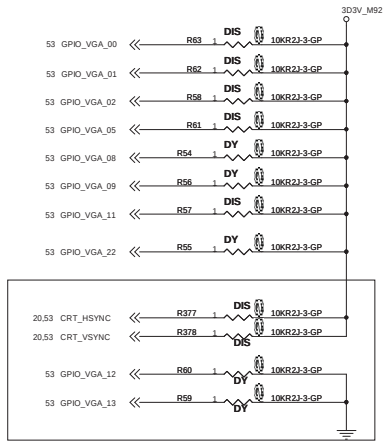
40.2R PN:64.40R25.6DL

(0.5 * VDDR1) (for SSTL-1.8/SSTL-2/DDR2)
(0.7 * VDDR1) (for GDDR3/GDDR4)

DIVIDER RESISTORS	DDR2	DDR3	GDDR3
MVREF TO 1.8V	100R	100R	40.2R
MVREF TO GND	100R	100R	100R







HDMI must only be enabled on systems that are legally entitled. It is the responsibility of the system designer to ensure that the system is entitled to support this feature.

STRAPS	PIN	DESCRIPTION
GPIO	DVPDATA(23:20) (Internal PD)	Initialization Behavior: This signal is input during reset (no reference clock is required). After reset, the default state is output low (0 V). The signals above can be left unconnected if not used.

AMD RESERVED CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

H2SYNC, GENERICC

PULLUP PADS ARE NOT REQUIRED FOR THESE STRAPS BUT IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

GPIO_28_TDO , GPIO21_BB_EN

If BIOS_ROM_EN (GPIO22) = 0		If BIOS_ROM_EN (GPIO22) = 1		
Size of the primary memory apertures	GPIO[13,12,11]	Manufacturer	Part Number	GPIO[13,12,11]
V 128MB	x000	ST Microelectronics	M25P05A	0100
256MB	x001		M25P10A	0101
64MB	x010		M25P20	0101
32MB	x		M25P40	0101
512MB	x		M25P80	0101
1GB	x			
2GB	x	Chingis (formerly PMC)	Pm25LV512A	0100
4GB	x		Pm25LV010A	0101

STRAPS	PIN	DESCRIPTION	RECOMMENDED SETTINGS 0= DO NOT INSTALL RESISTOR 1 = INSTALL 10K RESISTOR X = DESIGN DEPENDANT NA = NOT APPLICABLE
TX_PWRS_ENB (Internal PD)	GPIO0	PCIE FULL TX OUTPUT SWING Tansmitter Power Savings Enable 0= 50% Tx output swing 1= Full Tx output swing	1
TX_DEEMPH_EN (Internal PD)	GPIO1	Transmitter De-emphasis Enable 0= Tx de-emphasis disabled 1= Tx de-emphasis enabled	1
BIF_GEN2_EN_A	GPIO2	PCIE GNE2 ENABLED 0 = Advertises the PCI-E device as 2.5GT/s 1 = Advertises the PCI-E device as 5GT/s	1
AC_BATT	GPIO5	AC (Performance mode) = 3.3 V Battery saving mode = 0.0 V	
ROMSO	GPIO8	BIF_CLK_PM_EN Serial ROM Output from ROM	0
ROMSI	GPIO9	VGA ENABLED Serial ROM Input to ROM	0
ROMIDCFG[3:0] (Internal PD)	GPIO[13,12,11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT if BIOS_ROM_EN=1,then Config[3:0] defines the ROM type if BIOS_ROM_EN=0,then Config[3:0] defines the primary memory apeture size	X X X
PWRCNTL_[1,0]	GPIO[15,20]	Power control signals to control the core voltage regulator	
BB_EN	GPIO21	Back Bias (body bias) which minimizes power consumption in battery modes. 0V = Disable 3D3V = Enable	0
AUD[1] AUD[0] (Internal PD)	VGA_HSYNC VGA_VSYNC	AUD[1:0] 00:No audio function 01:Audio for DisplayPort and HDMI (if adapter is detected) 10:Audio for DisplayPort only 11:Audio for both DisplayPort and HDMI	1
CCBYPASS	GENERICC		0

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Title: Memory / Straps

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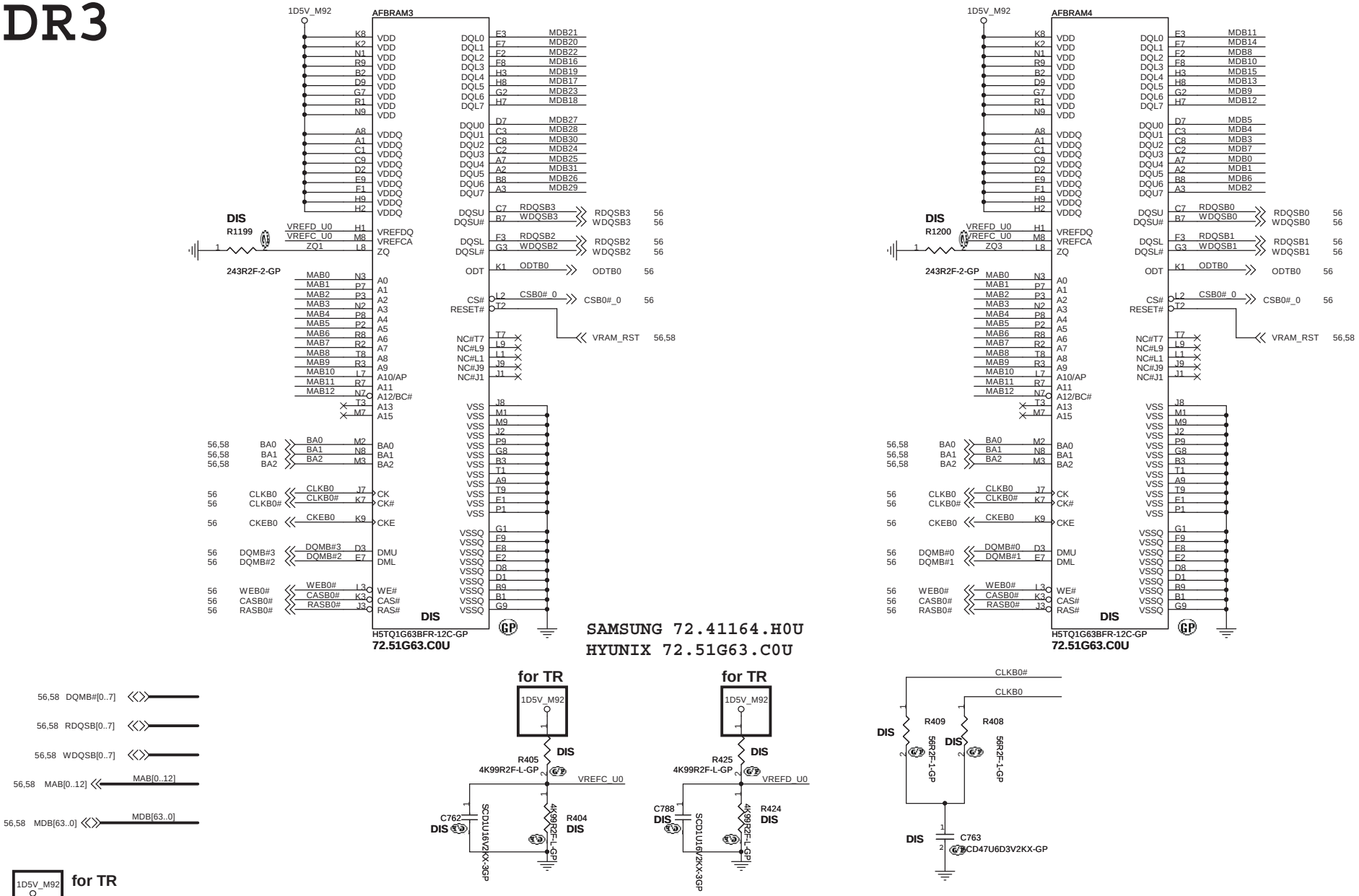
DDR3



UMA

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Title	DDR3 B0	
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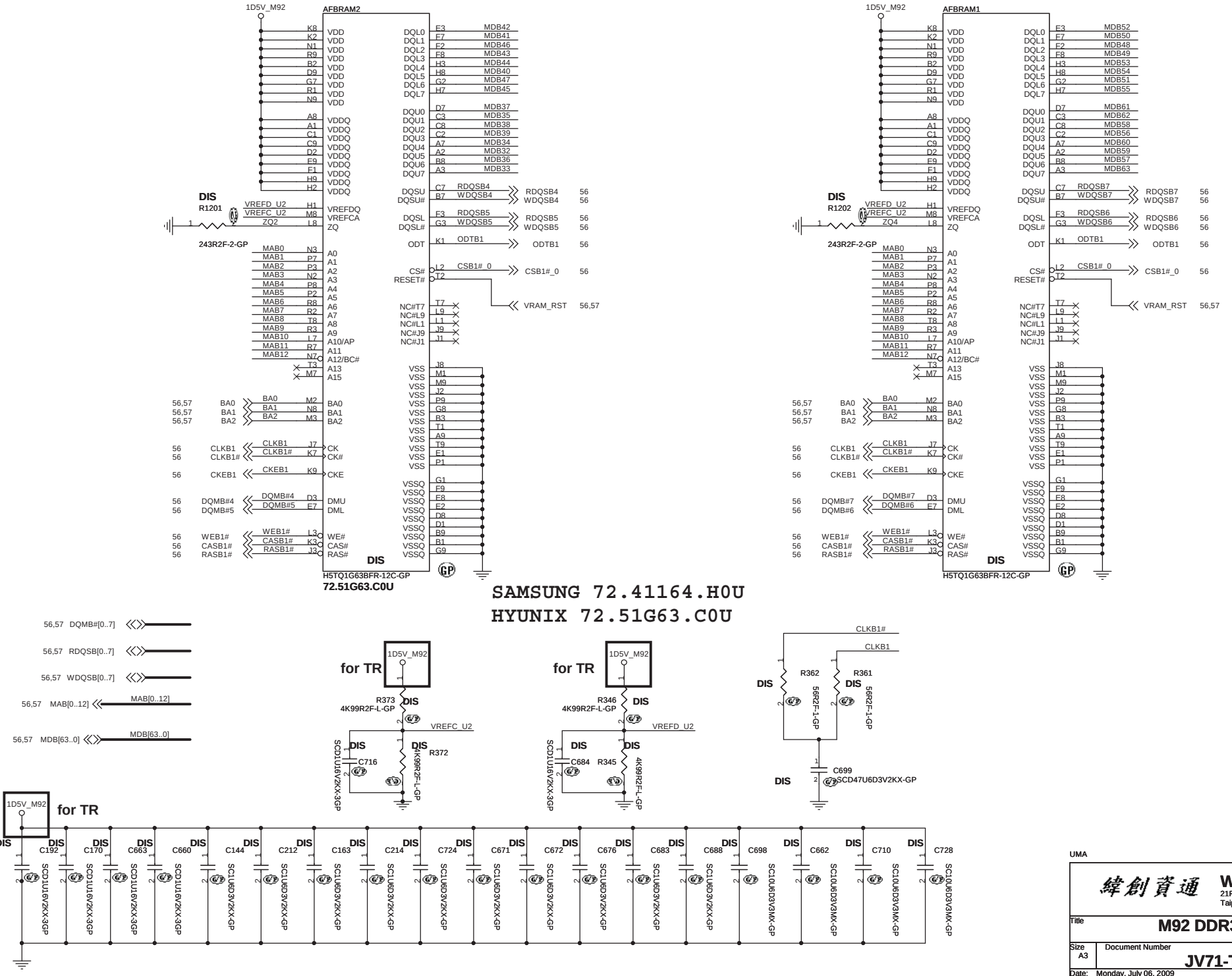

UMA

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Title: **M92 DDR3 B1**

Size: A3 | Document Number: **JV71-TR** | Rev: **SB**

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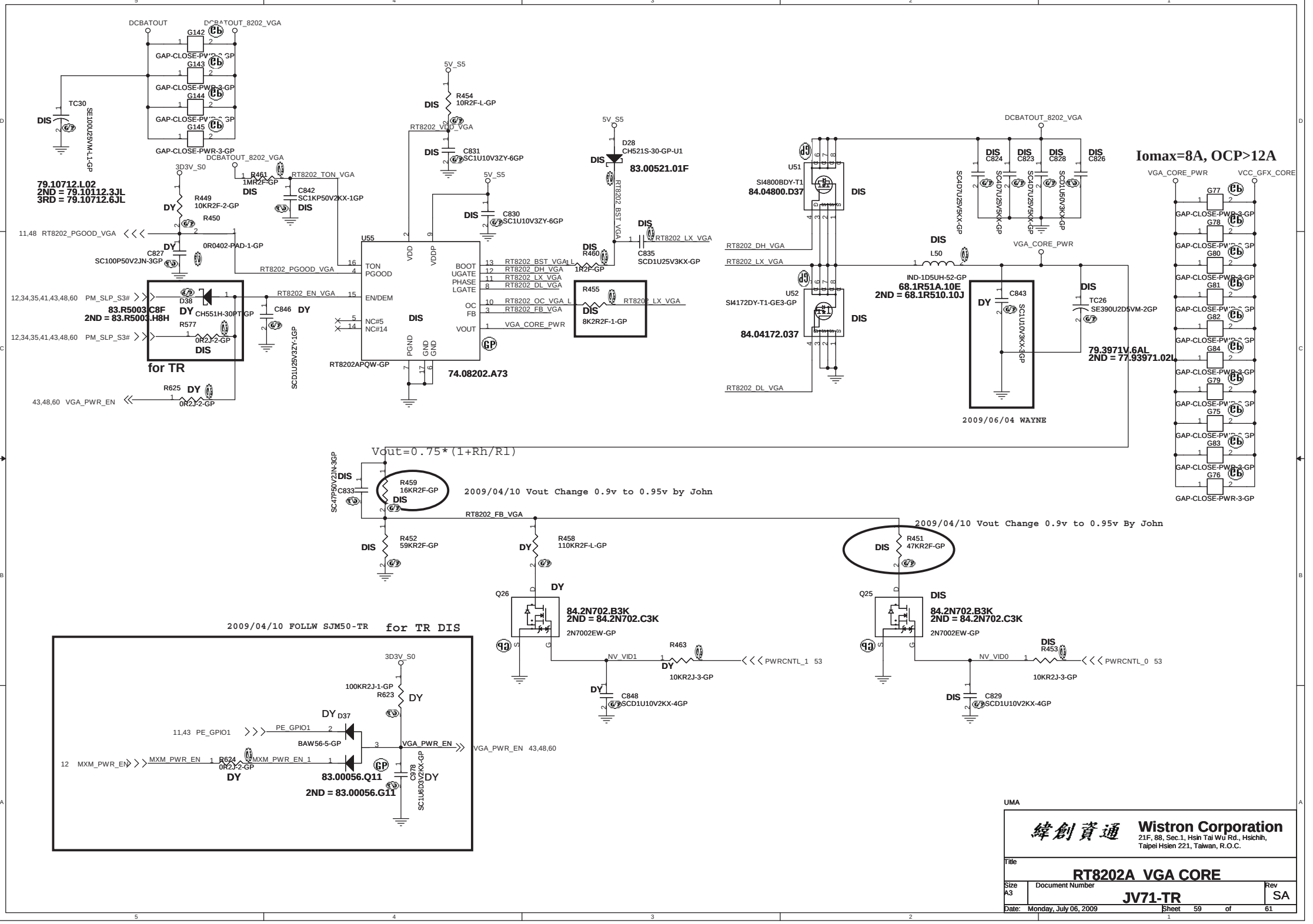
DCBATOUT
DCBATOUT_8202_VGA
G142
GAP-CLOSE-PWR-3-GP
G143
G144
G145
TC30
SE100U25VM-1-GP
79.10712.L02
2ND = 79.10112.3JL
3RD = 79.10712.6JL
3D3V_S0
R461
1MR2F-GP
RT8202_TON_VGA
C842
SC1KP50V2KX-1GP
R449
10KR2F-2-GP
R450
0R0402-PAD-1-GP
11,48 RT8202_PGOOD_VGA
C827
SC100P50V2JN-3GP
12,34,35,41,43,48,60 PM_SLP_S3#
D38
CH551H-30PT-GP
83.R5003.C8F
2ND = 83.R5003.H8H
C846
R577
0R2J-2-GP
for TR
R625
0R2J-2-GP
43,48,60 VGA_PWR_EN
SCD1U25V3ZY-1GP
5V_S5
R454
10R2F-L-GP
RT8202_VDD_VGA
C831
SC1U10V3ZY-6GP
C830
SC1U10V3ZY-6GP
U55
TON
PGOOD
VDD
VDDP
EN/DEM
NC#5
NC#14
PGND
GND
BOOT
UGATE
PHASE
LGATE
OC
FB
VOUT
RT8202_BST_VGA
RT8202_DH_VGA
RT8202_LX_VGA
RT8202_DL_VGA
RT8202_OC_VGA_L
RT8202_FB_VGA
VGA_CORE_PWR
RT8202_EN_VGA
RT8202APQW-GP
74.08202.A73
D28
CH521S-30-GP-U1
83.00521.01F
RT8202_BST_VGA
R460
1R2F-GP
C835
SCD1U25V3KX-GP
R455
8K2R2F-1GP
U51
SI4800BDY-T1
84.04800.D37
U52
SI4172DY-T1-GE3-GP
84.04172.037
L50
IND-1D5UH-52-GP
68.1R51A.10E
2ND = 68.1R510.10J
C824
C823
C828
C826
SC4D7U25V5KX-GP
SCD1U50V3KX-GP
C843
SC1U10V3KX-GP
TC26
SE390U2D5VM-2GP
79.3971V.6AL
2ND = 77.93971.02L
2009/06/04 WAYNE
Iomax=8A, OCP>12A
VGA_CORE_PWR
VCC_GFX_CORE
G77
G78
G80
G81
G82
G84
G79
G75
G83
G76
GAP-CLOSE-PWR-3-GP
Vout=0.75*(1+Rh/R1)
SC47P50V2JN-3GP
C833
R459
16KR2F-GP
2009/04/10 Vout Change 0.9v to 0.95v by John
R452
59KR2F-GP
R458
110KR2F-L-GP
R451
47KR2F-GP
2009/04/10 Vout Change 0.9v to 0.95v By John
Q26
84.2N702.B3K
2ND = 84.2N702.C3K
2N7002EW-GP
Q25
NV_VID1
NV_VID0
R463
10KR2J-3-GP
R453
PWRCNTL_1 53
PWRCNTL_0 53
C848
SCD1U10V2KX-4GP
C829
SCD1U10V2KX-4GP
2009/04/10 FOLLW SJM50-TR
for TR DIS
3D3V_S0
100KR2J-1-GP
R623
D37
BAW56-5-GP
11,43 PE_GPIO1
PE_GPIO1
VGA_PWR_EN
VGA_PWR_EN 43,48,60
12 MXM_PWR_EN
MXM_PWR_EN
MXM_PWR_EN_1
R624
0R2J-2-GP
83.00056.Q11
2ND = 83.00056.G11
C978
SC1U6D3V2KX-GP
DIS
DY
UMA
緯創資通
Wistron Corporation
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Title
RT8202A VGA CORE
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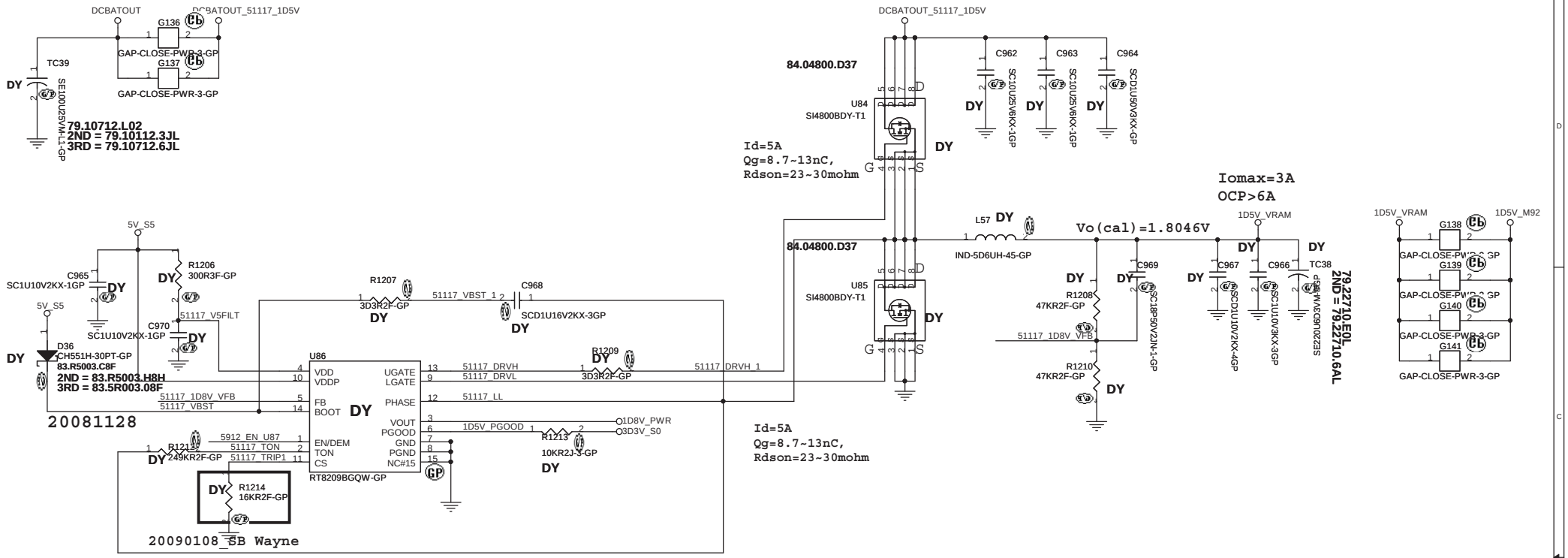

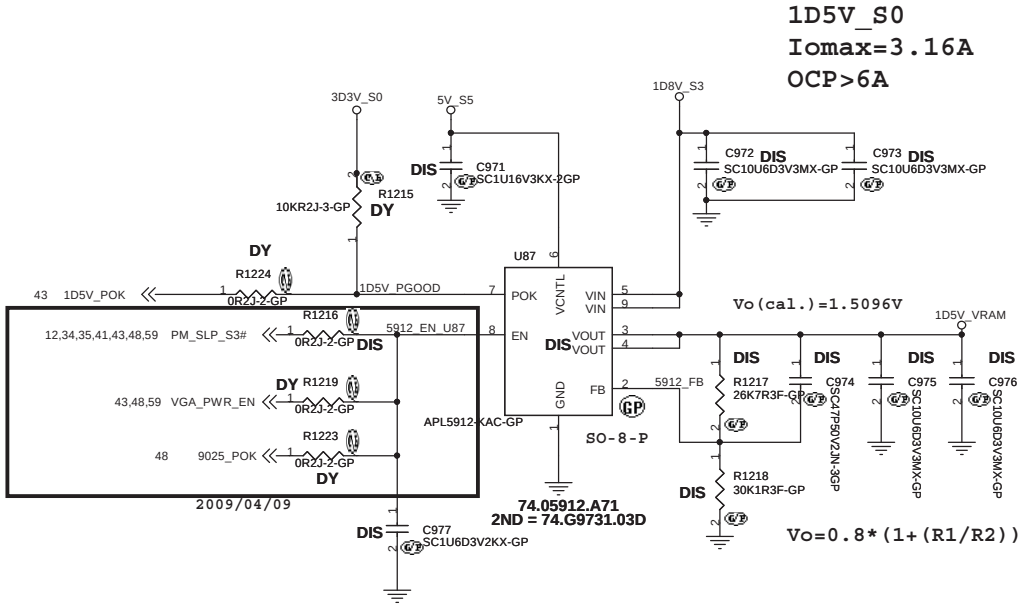

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Title	***RT8209B/APL5912_1D5V_ VRAM***	
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HISTORY

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